Immersion 800G OSFP DR8 Optical Transceiver Module for liquid cooling

P/N: FQU-800P4M50XXX

Features

- ✓ OSFP MSA and CMIS compliant
- ✓ 8x106.25Gbps (53.125GBd PAM4) electrical interface
- ✓ 8x106.25Gbps (53.125GBd PAM4) optics architecture
- ✓ Power consumption <15W
- ✓ Up to 500m G.652 SMF with KP-FEC
- ✓ Support pluggable dual MPO-12 pigtails
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant (lead free)

Applications

- ◆ 800GBASE-DR8
- ◆ AI/ML Application
- ◆ Data center network
- ◆ Especially design for liquid immersion environment

Description

The FIBERSTAMP 800G OSFP DR8 is a transceiver module designed for optical communication applications of up to 500 m in liquid immersion environments. It is built on two core technological pillars—advanced silicon photonics chips and a state-of-the-art 5 nm DSP—working in synergy to deliver exceptional performance, efficiency, and integration.

Specifically engineered for liquid immersion, the module's housing is sealed with a protective coating to prevent coolant ingress into the optical engine. Compared with other liquid-immersion optical solutions, this design incorporates a dedicated pressure test point for leakage detection, giving the sealing and testing process a unique advantage in manufacturing quality assurance.

Built to withstand the most demanding operating conditions, the module resists extreme temperatures, high humidity, and EMI interference. It also offers extensive functionality and feature integration, all accessible via a two-wire serial interface.

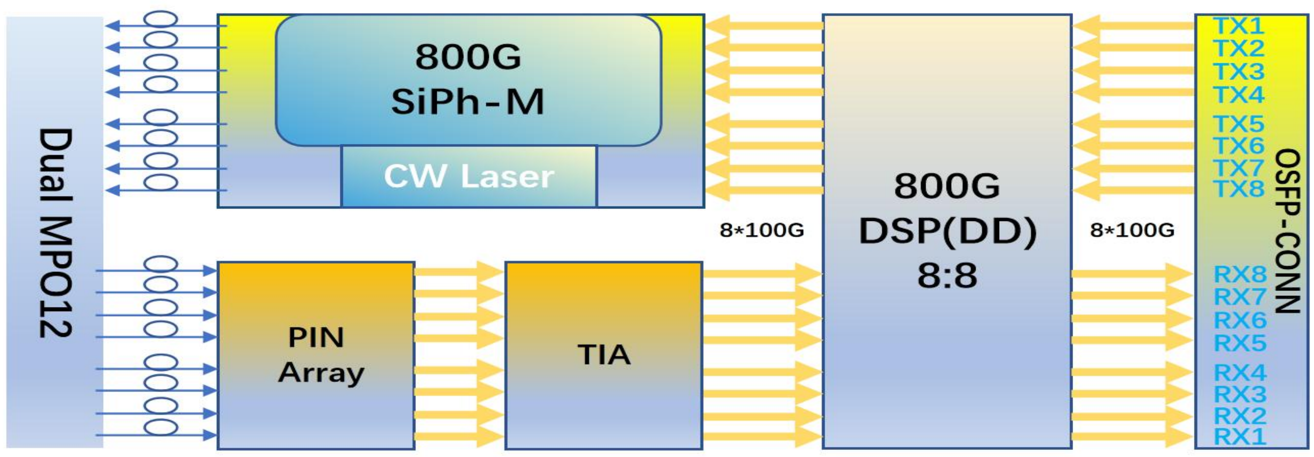


Figure1. DR8 Module Block Diagram

Advantage

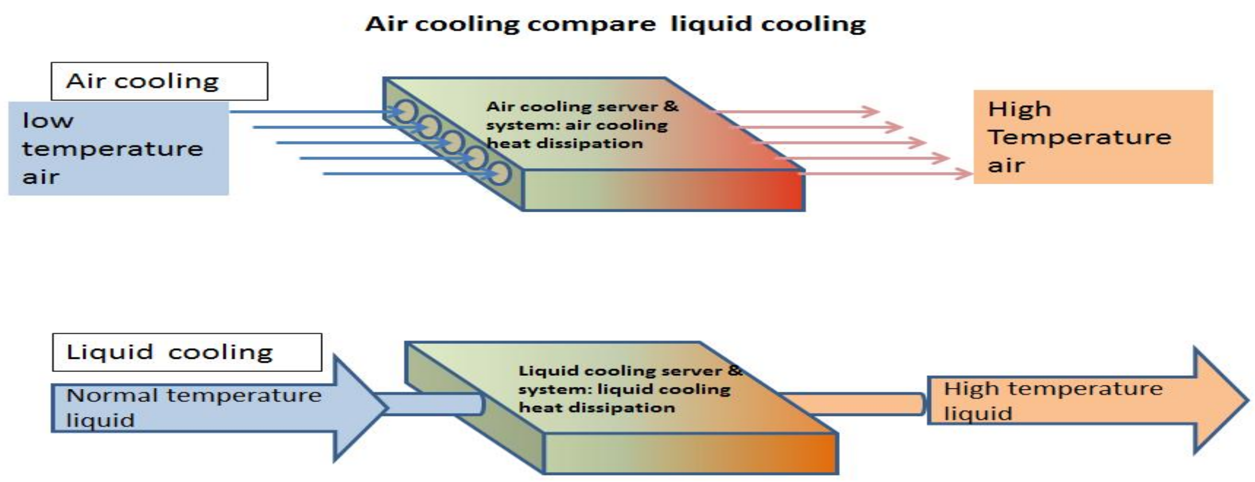


Figure 2. Liquid cooling advantage

As the requirement of data traffic keeping growth and the heat flux emitted by datacenter internal chips increases constantly, traditional air cooling methods are under pressure. Liquid cooling technologies removes the heat more efficiently with dielectric fluids that have high heat capacity to improve the efficiency of energy in datacenter. FIBERSTAMP solved the lack of optical transceivers which perform reliability in immersion even liquid immersion depth up to 10m, the Liquid cooling optical series transceiver is suitable for liquid cooling server & system, this series product are compatible with fluorinated liquid and mineral oils well.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane	fd		106.25		Gbit/s
Humidity	Rh	5		85	%
Power Dissipation	Pm			15	W
Fiber Bend Radius	Rb	3			cm
Liquid immersion depth	Dp			10	M

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	400		900	mVp-p
Differential output voltage amplitude	ΔVout			850	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	V_{IH}	2.0		V_{CC}	V

Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{CC}-0.5		V_{CC}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note：

1) BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2) Differential input voltage amplitude is measured between TxnP and TxnN.
3) Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	1304.5		1317.5	nm	-
Side-mode suppression ratio	SMSR	30	-	--	dB	-
Average launch power, each lane	Pout	-2.9	-	4.0	dBm	-
Optical Modulation Amplitude(OMA outer), each lane	OMA	-0.8	-	4.2	dBm	-
Transmitter and dispersion eye closure for PAM4 (TDECQ),each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-16	dB	-
Receiver						
Centre Wavelength	λc	1304.5		1317.5	nm	-
Receiver Sensitivity in OMA outer Note1	RXsen			-4.4	dBm	1
Average power at receiver , each lane input, each lane	Pin	-5.9		4	dBm	-
Receiver Reflectance				-26	dB	-
LOS Assert		-15	-13		dBm	-
LOS De-Assert			-11	-9	dBm	-
LOS Hysteresis		0.5			dB	-

Note：

1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin List and Description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

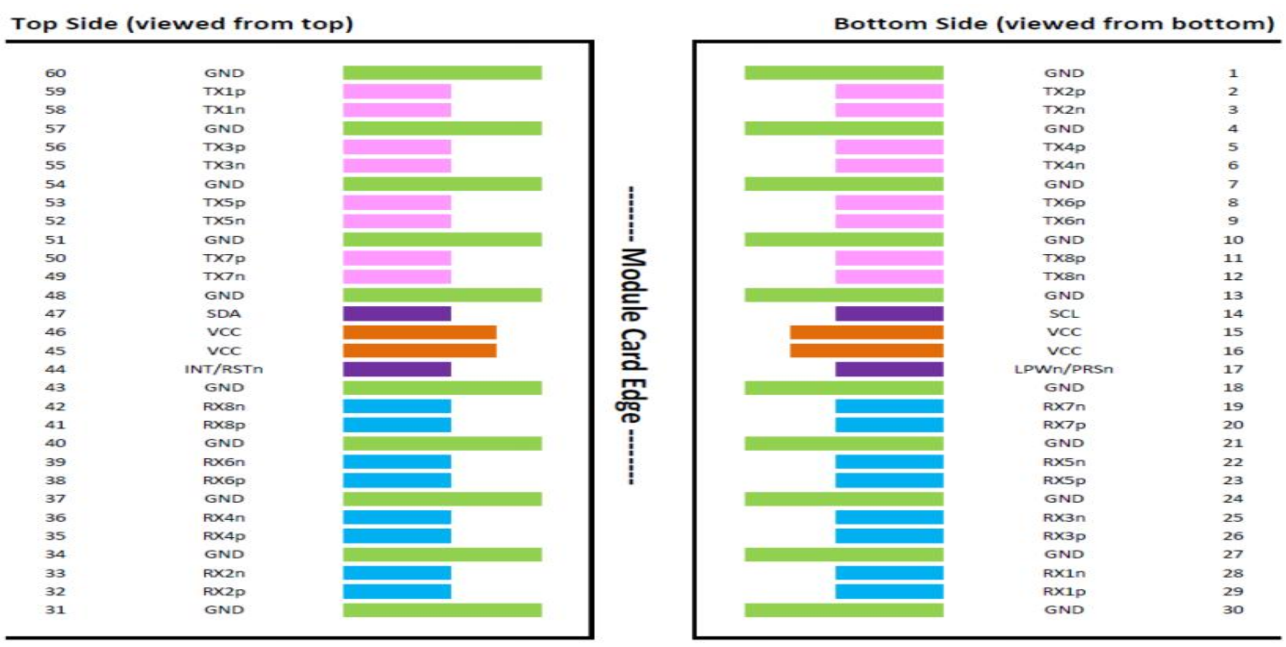


Figure3. OSFP module Pin-out Details

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 4 enables multi level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active high signal on the module which gets translated to an active-high signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 3 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INT signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

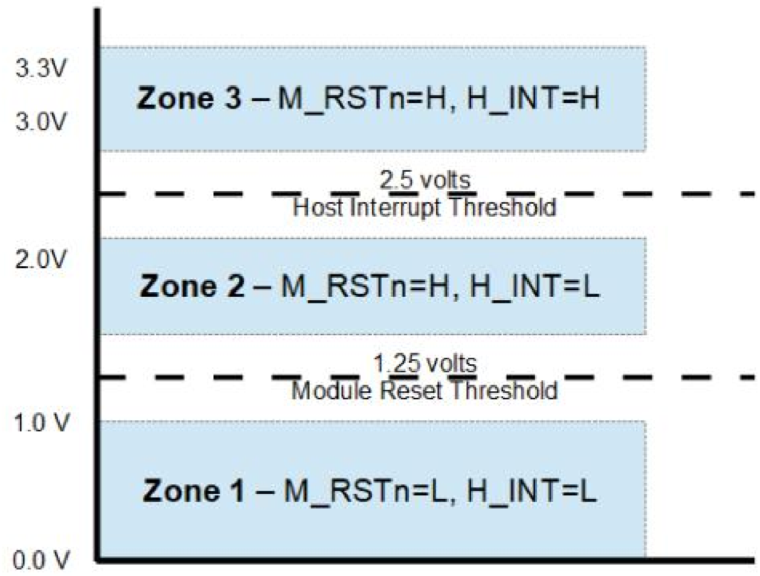


Figure4. INT/RSTn voltage zones

• Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INT=Low). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 1.

• Zone 2 – Normal operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INT=Low). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 1.

• Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INT=High). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 1.

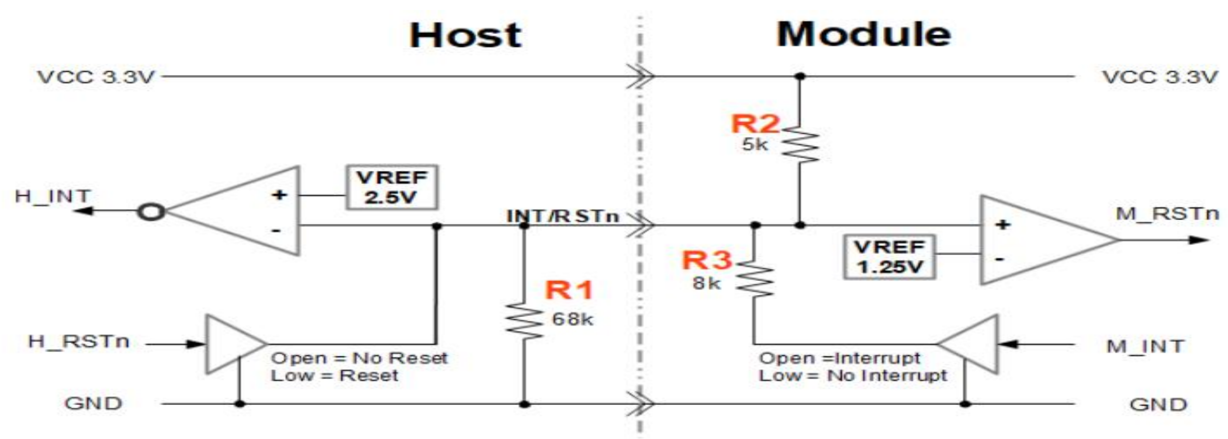


Figure 5. INT/RSTn circuit

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INT	2.500	2.475	2.525	Volts	Precision voltage reference for H_INT
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

Table 1. INT/RSTn circuit parameters

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 6 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an activelow signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 5 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

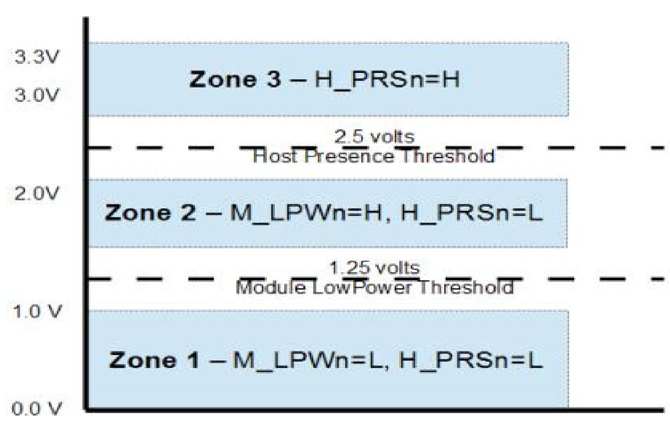


Figure 6. LPWn/PRSn voltage zones

• Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 2.

• Zone 2 – High Power mode – Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 2.

• Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 2.

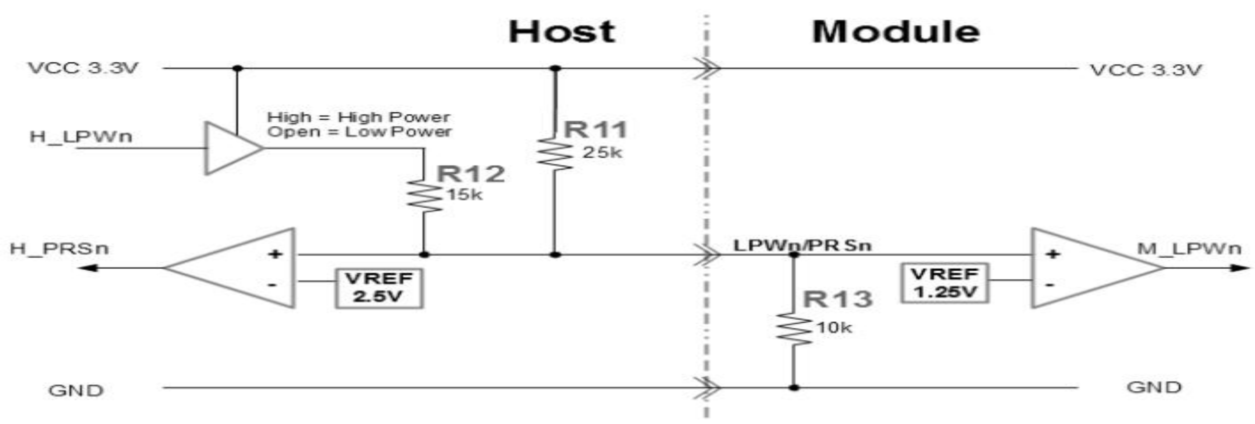


Figure 7. LPWn/PRSn circuit

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

Table 2. LPWn/PRSn circuit parameters

Power Supply Filtering

Figure 7 provides an example implementation for a 3.3V power filter on the host board.
If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

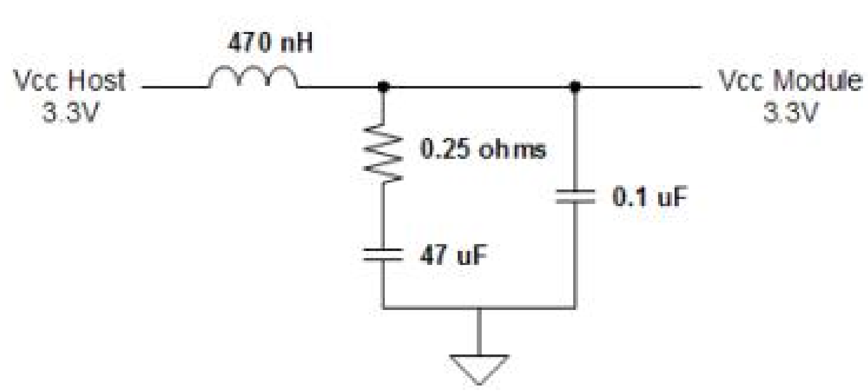


Figure8. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FIBERSTAMP OSFP products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

The TWI protocol only supports eight-bit addresses. This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper

Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 8. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

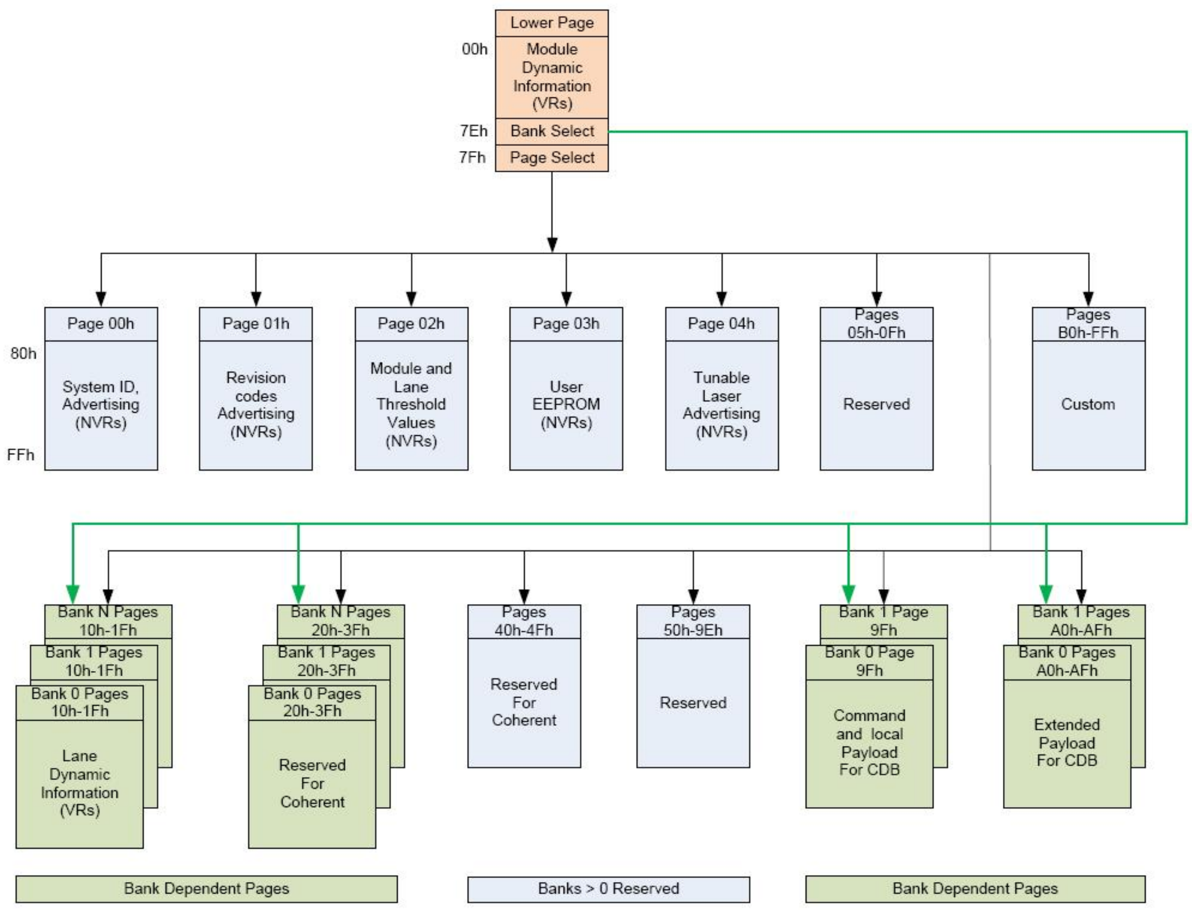
Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.



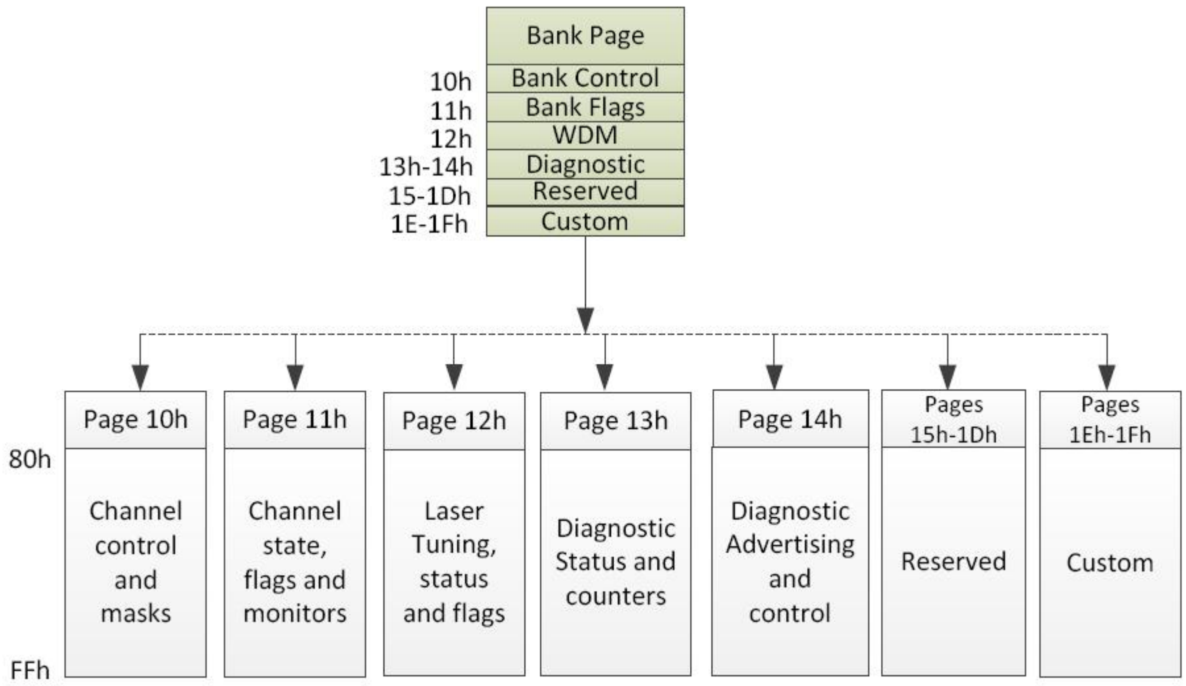


Figure9. OSFP Memory Map

Mechanical Dimensions(mm)

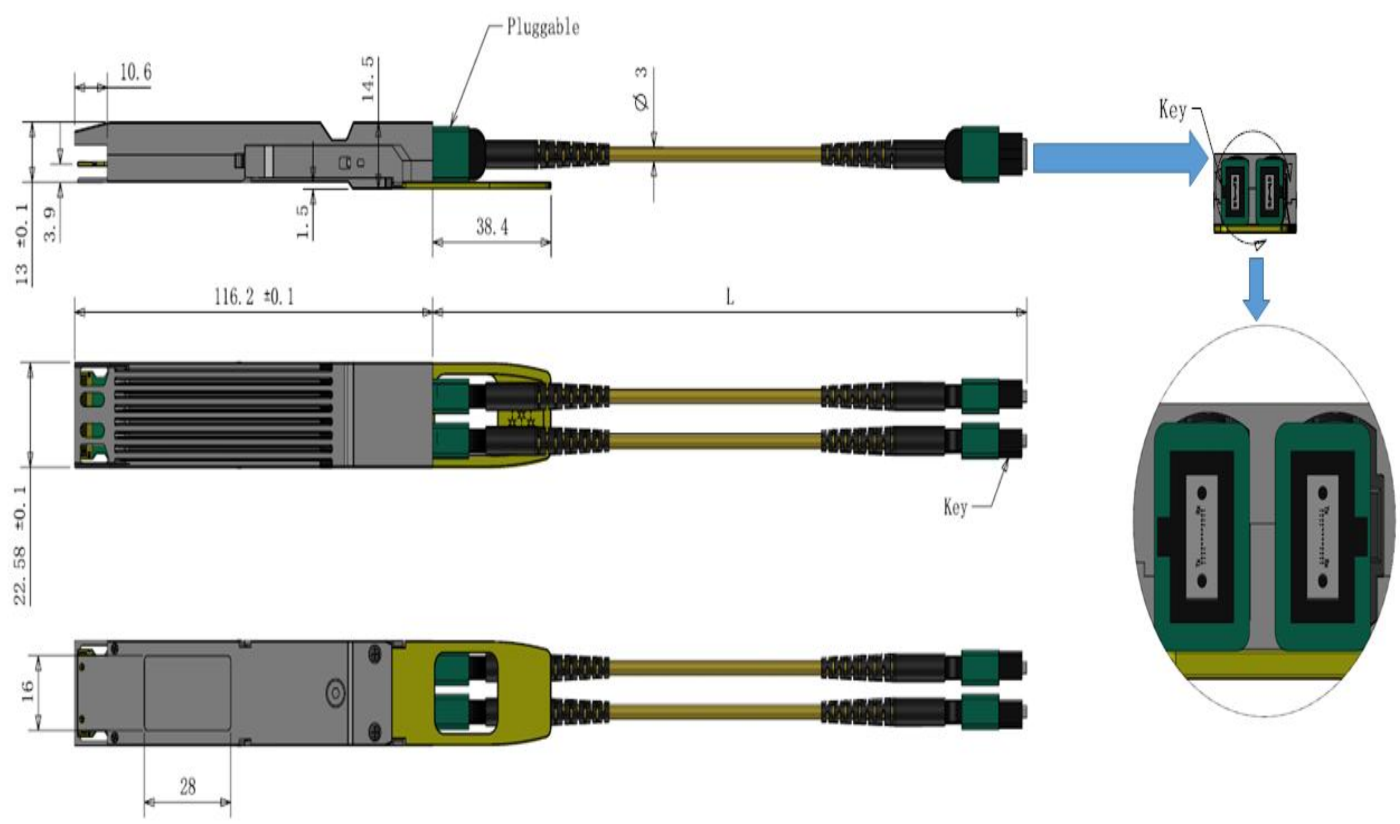


Figure10. Mechanical Specifications

Regulatory Compliance

FIBERSTAMP FQU-800P4M50XXX transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. OSFP MSA
2. CMIS 5.x
3. IEEE802.3
4. OIF CEI-112G-VSR

⚠**CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FQU-800P4M50XXX	800G OSFP DR8 transceiver, pluggable dual MPO-12 pigtails for liquid immersion, up to 500m on Single mode Fiber (SMF).

Important Notice

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Revision History

Revision	Date	Description
V0	Aug-05-2025	Advance Release.