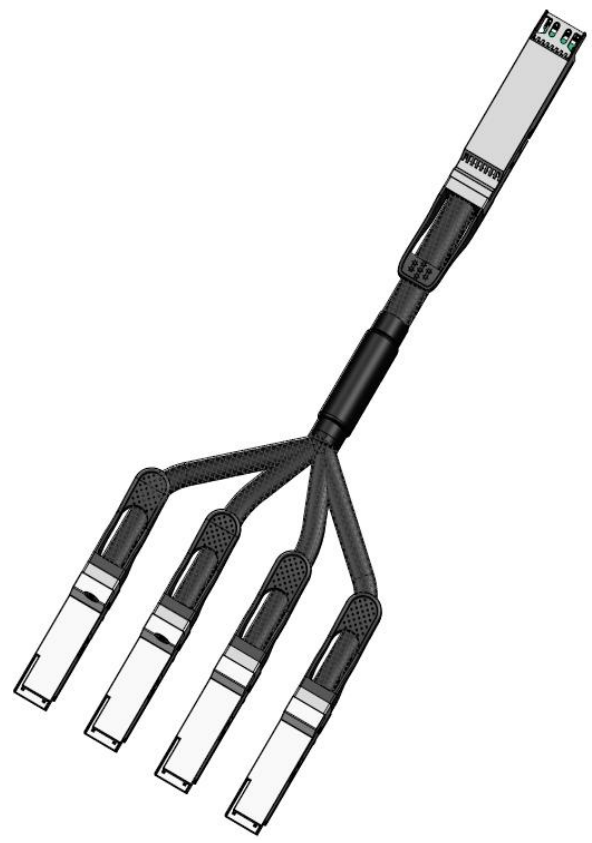
800G OSFP to 4x200G QSFP112 Breakout Active Copper Cable

P/N: FWU4J-800xxxxxC

Features

- ✓ Hot-plug OSFP CTHS and QSFP112 form factor
- ✓ Support 8x 50/100Gb/s PAM4 modulation with 16 pairs
- ✓ Support up to 5m length
- ✓ 100Ohm differential impedance system
- ✓ 3.3V power supply & typical power consumption 3.5W
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ I2C management



Applications

- ✓ Infiniband NDR/HDR/EDR
- ✓ Switch / router / HBA
- ✓ Enterprise network
- ✓ Data Center Network
- ✓ Data storage and communication industry

STANDARDS COMPLIANCE

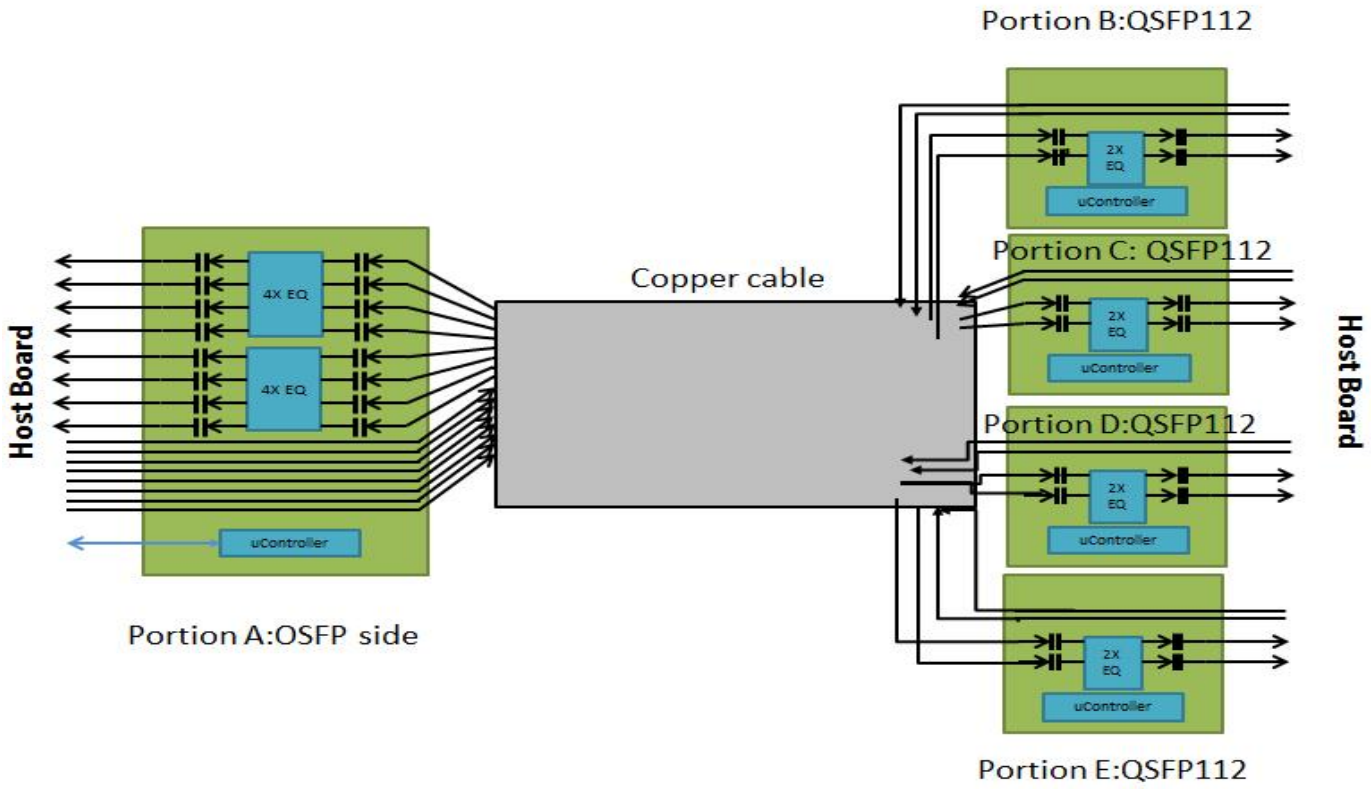
- ✓ IEEE P802.3ck D3.0
- ✓ QSFP-DD MSA HW Rev 4.1
- ✓ QSFP112 MSA HW Rev 6.01
- ✓ CMIS 4.0
- ✓ RoHS

Description

FIBERSTAMP's ACC(Active Copper Cable) assembly series product provide superior signal integrity performance and reliability, comparing to PCC and AOC, ACC is a re-drive solution which built-in linear equalizer to compensate transmission loss, it is an effective solution with low power, low latency, low cost to help high-speed data centers even AI high-computational applications.

FIBERSTAMP's FWU4J-800xxxxxC cable connects data signals from each of the 16 pairs on the single OSFP end to the quad QSFP112 ends, each pair operates at data rates of up to 100Gb/s and can be adaptive downward compatibility. The product operates 3.3V power supply and comply with OSFP-MSA and IEEE802.3ck ,it's high performance & cost effective I/O solutions for LAN, HPC and SAN.

Block Diagram



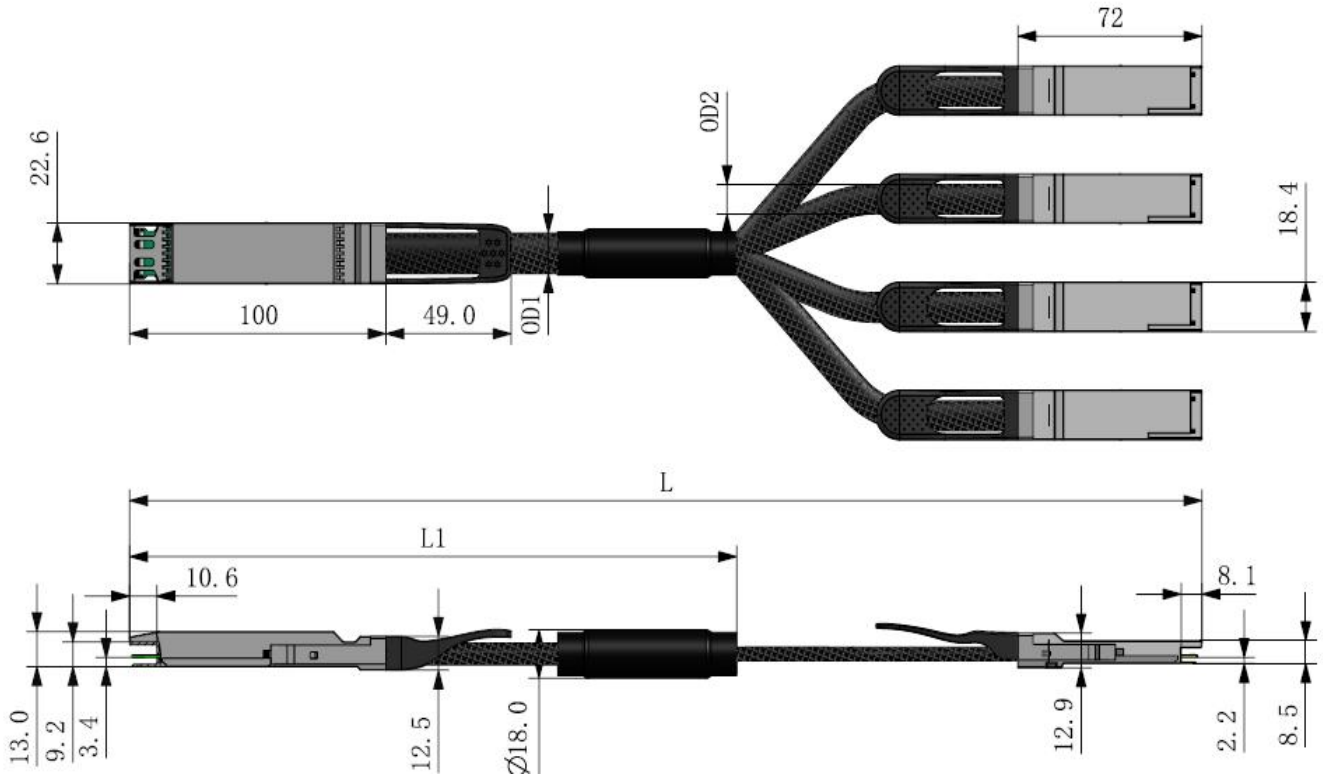
Absolute Maximum Ratings

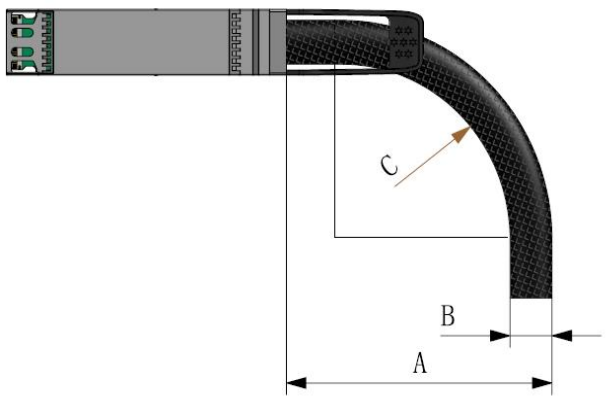
Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_s	-20	85	°C
Humidity(non-condensing)	Rh	5	95	%
Supply Voltage	Vcc	-0.3	3.6	V

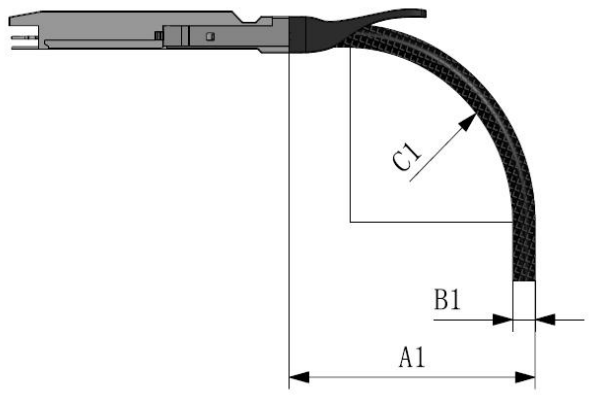
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_C	0		70	°C
Supply Voltage	Vcc	3.13	3.3	3.47	V
Power consumption	Pd		2.5		W
Data Rate per lane(PAM4)	Fd1		53.125		GBaud/s
Data Rate per lane(NRZ)	Fd2	10.3125	53.125		Gbps
Humidity	Rh	5		85	%

Mechanical Dimensions



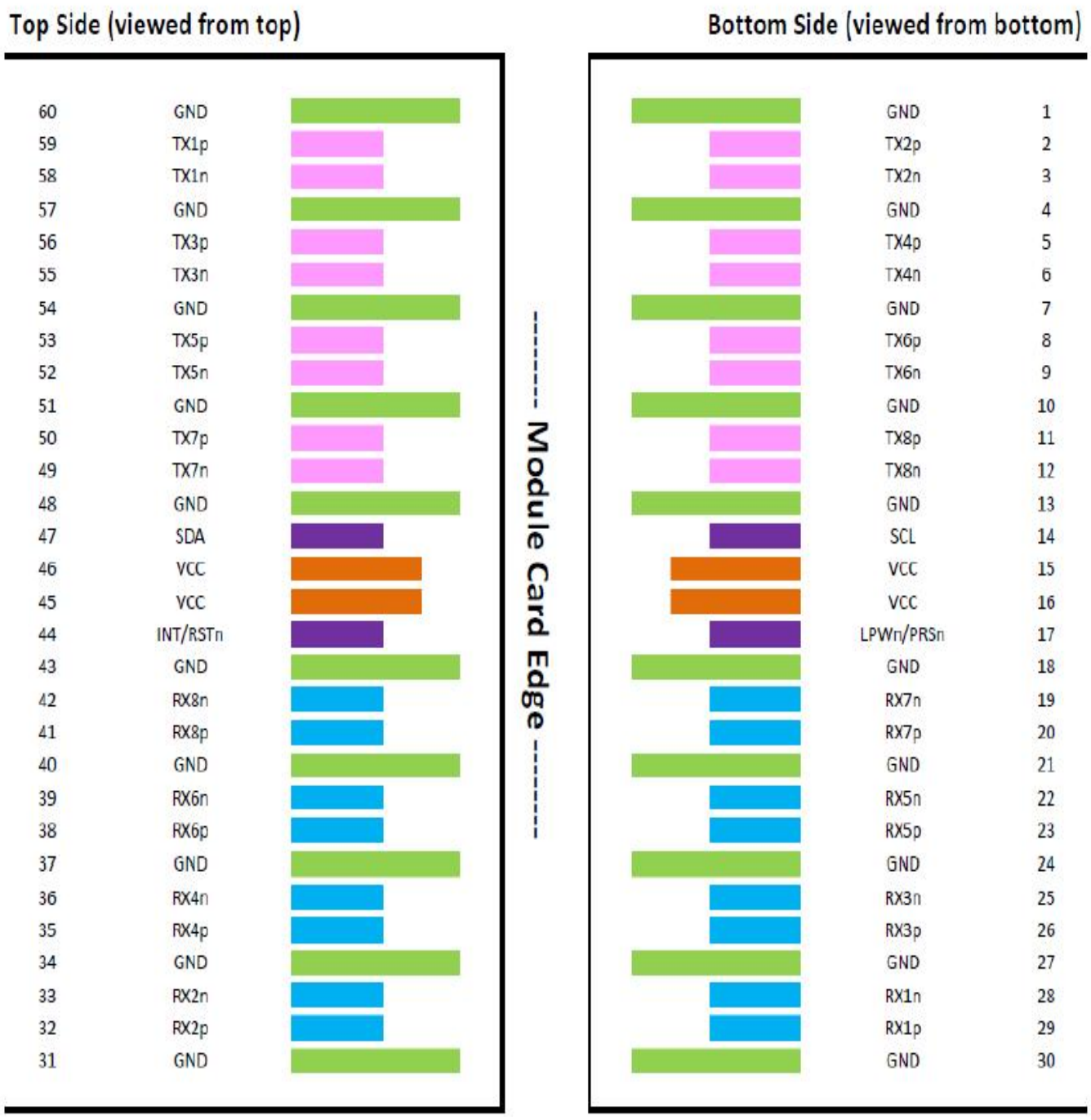




OSFP Horizontal Direction			
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"
26AWG	11MM	55MM	65MM

QSFP112 Vertical Direction			
CABLE GUAGE	DIAMETER"B1"	MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"
26AWG	8MM	40MM	50MM

OSFP Electrical pinout

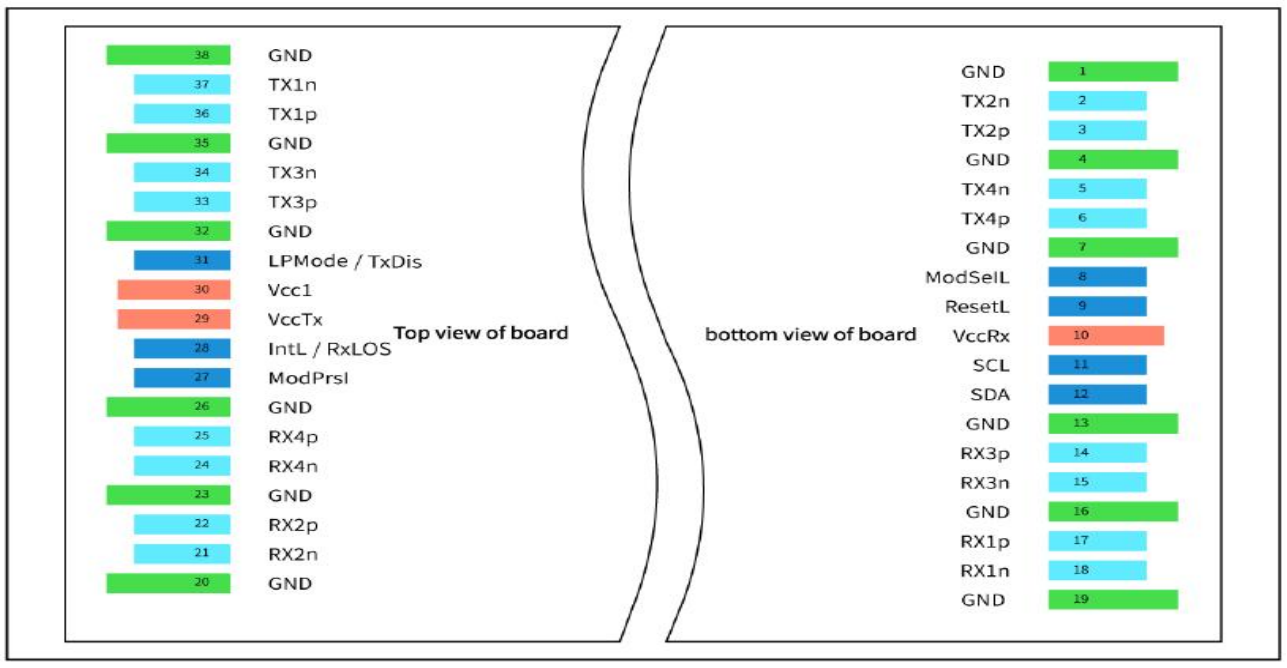


OSFP Electrical pin list and description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

QSFP112 Electrical pinout



QSFP112 Electrical pin list and description

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3	
12	LVCMOS-I/O	SDA	TWI serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Ordering information

Part Number	FWU4J-800xxxxxC
Length (meter)	2~5
Wire gauge (AWG)	AWG30/26

If length(meter) is decimal, PN should be as GOS-4QA801-DXXC,the wire gauge also can be customized. It's recommend to choose FIBERSTAMP's OSFP 800G DAC for less than 2m reach.

Important Notice

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Revision History

Revision	Date	Description
Preliminary	Aug-06-2024	Advance Release.