



800G OSFP to 4x200G OSFP RHS breakout Direct Attach Cable

P/N: FWU4U-800xxxxxC

Features

- ✓ Hot-plug OSFP CTHS and OSFP RHS form factor
- ✓ Support 8x 50/100Gb/s PAM4 modulation
- ✓ Commercial case temperature range of 0°C to 70°C
- √ 26 AWG ~30 AWG support up to 2m length above
- ✓ Contain EEPROM & programmable to customized

Applications

- ✓ Data storage and communication industry
- ✓ Switch / Router / HBA/NIC
- ✓ Enterprise network
- ✓ Data Center Network
- ✓ Infiniband



- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA HW Rev 4.1
- ✓ ROHS



Description

FIBERSTAMP's 800G OSFP to 4x200G OSFP cable assembly splitter is effective alternative to fiber optics. The cable connects data signals from each of the 16 pairs on the single OSFP end to the quad OSFP RHS ends, each pair operates at data rates of up to 100Gb/s, each OSFP/OSFP RHS port can be addressed by EEPROM to provide product information, which can be read or write by I2C interface.

FIBERSTAMP's FWU4U-800xxxxxC cable assembly splitter is compliant with the OSFP-MSA and IEEE 802.3ck, it's a high performance, lowest-cost &latency &power consumption I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 800 Gigabit Ethernet, InfiniBand EDR /HDR/NDR and temperature requirements for performance and reliability.

The height of OSFP CTHS (Close Top Heat Sink) is fully compliant with OSFP finned top, OSFP RHS(Riding Heat Sink) also can be called flat top, it's a little bit lower than OSFP CTHS.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	T _c	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

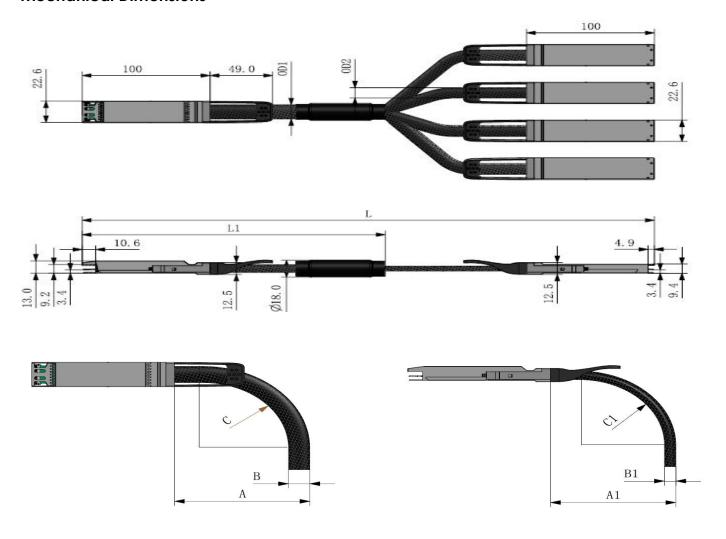
Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	°C
Baud Rate per Lane (PAM4)	fd		53.125		GBaud/s
Humidity	Rh	5		85	%







Mechanical Dimensions



OSFP Horizontal Direction				
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"	
26AWG	11MM	55MM	65MM	

OSFP RHS Vertical Direction			
CABLE GUAGE DIAMETER"B1"		MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"
26AWG	8MM	40MM	50MM

OSFP Electrical pinout

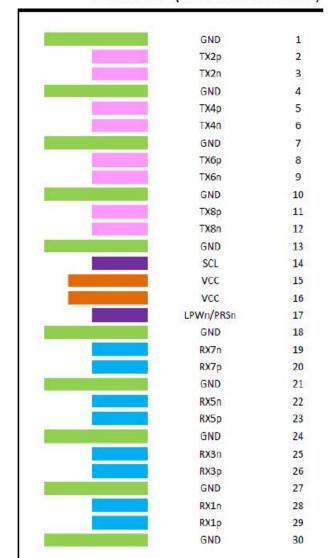




Top Side (viewed from top)

0	GND	
9	TX1p	
8	TX1n	
57	GND	
6	TX3p	
5	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
19	TX7n	
18	GND	
17	SDA	
6	VCC	
15	VCC	1
14	INT/RSTn	
13	GND	
12	RX8n	
11	RX8p	
10	GND	
39	RX6n	
88	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

Bottom Side (viewed from bottom)



Electrical pin list and description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground		22	1	
8	ТХбр	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pul up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground		5	1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground		_	1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	





Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	vcc	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground		7	1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	ĺ
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Ordering information

Part Number	GQD-PC801-XXXC		
Length (meter)	0.5	1	2
Wire gauge (AWG)	30	30	26

If length(meter) is decimal, PN should be as GOS-4OP801-DXXC, above 2m reach also can be customized.

Important Notice

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Revision History

Revision	Date	Description
VO	Jun-21-2024	Advance Release.