800G-CR8 (OSFP RHS) Active Copper Cable

P/N: FZU-800-XXM02C

Features

- ✓ Hot-plug OSFP RHS form factor
- ✓ Support 8x 100Gb/s PAM4 and NRZ
- ✓ Support up to 5m length
- ✓ 100Ohm differential impedance system
- ✓ 3.3V power supply & typical power consumption 2.5W
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ I2C management

Applications

- ✓ Infiniband NDR/HDR/EDR
- ✓ Switch / router / HBA
- ✓ Enterprise network
- ✓ Data Center Network
- ✓ Data storage and communication industry

STANDARDS COMPLIANCE

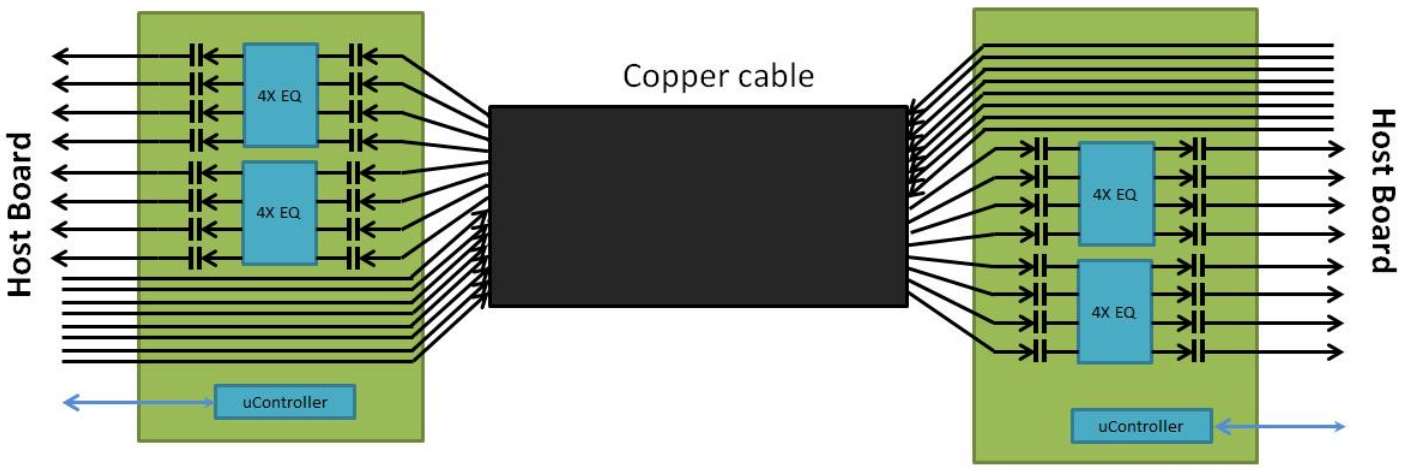
- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA R4.1
- ✓ CMIS 4.0
- ✓ ROHS

Description

FIBERSTAMP’s OSFP RHS ACC(Active Copper Cable) assembly series product provide superior signal integrity performance and reliability, comparing to PCC and AOC, ACC is a re-drive solution which built-in linear equalizer to compensate transmission loss, it is an effective solution with low power, low latency, low cost to help high-speed data centers even AI high-computational applications.

FIBERSTAMP’ s FZU-800-XXM02C cable connects data signals from each of the 16 pairs on the single OSFP RHS end to the other OSFP RHS end, each pair operates at data rates of up to 100Gb/s and can be adaptive downward compatibility. The product operates 3.3V power supply and comply with OSFP MSA and IEEE802.3ck ,it’ s high performance & cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet 400Gigabit Ethernet, Infiniband requirements for performance and reliability.

Block Diagram



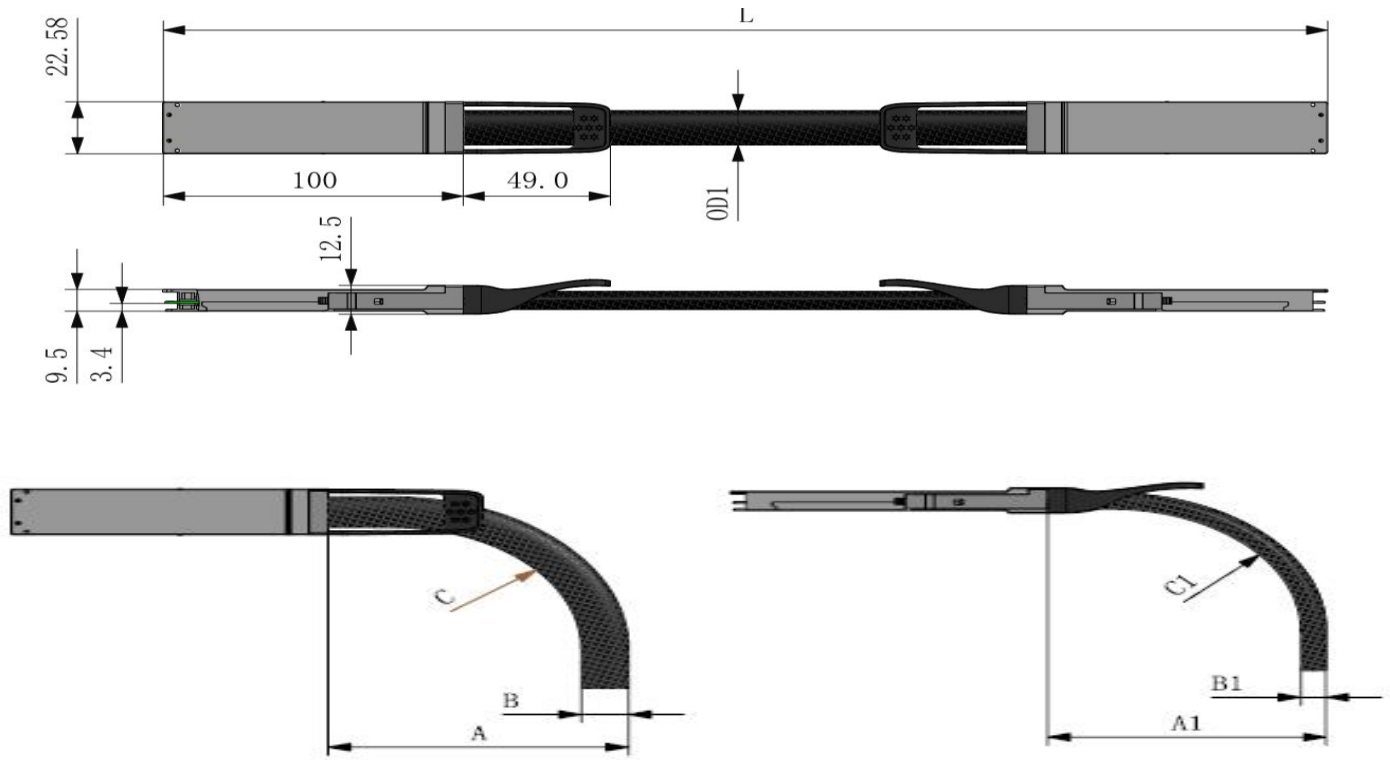
Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_s	-20	85	ºC
Humidity(non-condensing)	Rh	0	70	ºC
Supply Voltage	Vcc	-0.3	3.6	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_c	0		70	ºC
Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Consumption	PD		1.3		W
Data Rate per Lane (PAM4)	Fd1		53.125		GBaud/s
Data Rate per Lane (NRZ)	Fd2	10.3125	53.125		Gbps
Humidity	Rh	5		85	%

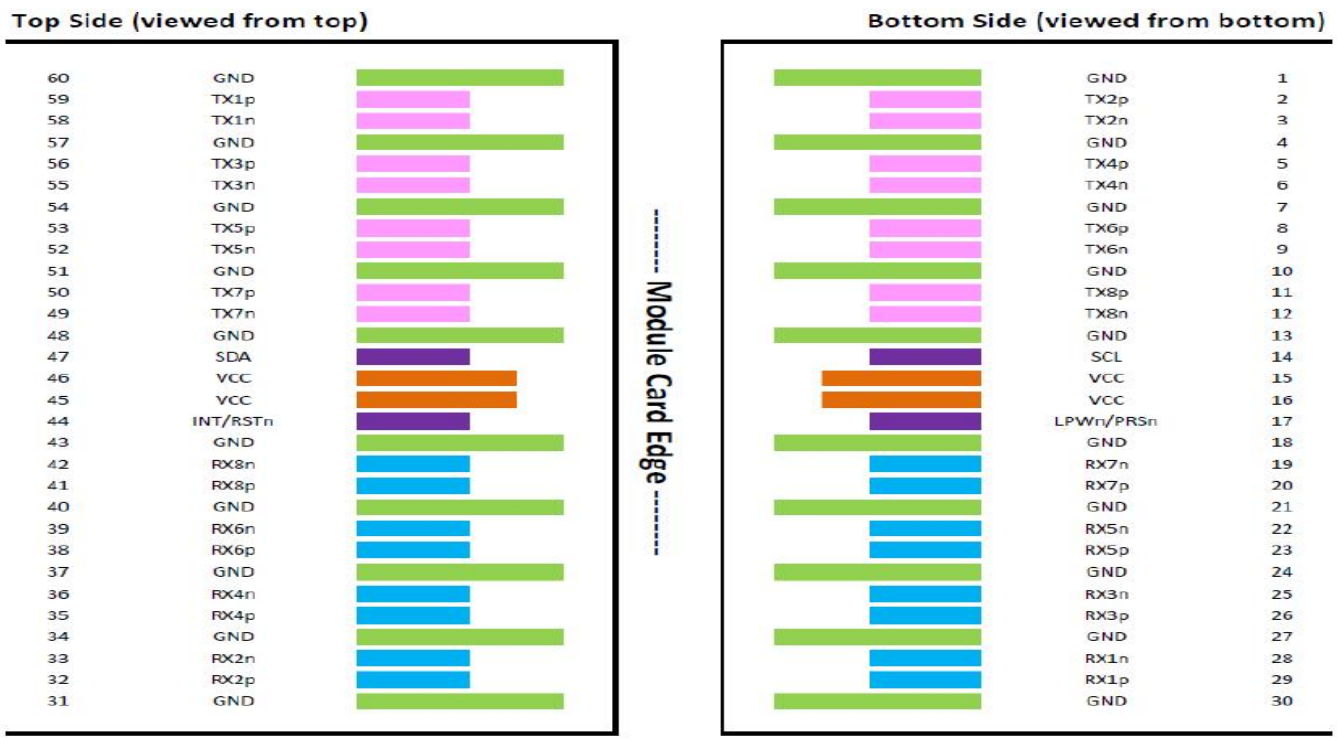
Mechanical Dimensions



OSFP RHS Horizontal Direction			
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"
26AWG	11MM	55MM	65MM

OSFP RHS Vertical Direction			
CABLE GUAGE	DIAMETER"B1"	MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"
26AWG	8MM	40MM	50MM

Electrical pinout



Electrical pin list and description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Ordering information

Part Number	FZU-800-XXM02C
Length (meter)	2~5
Wire gauge (AWG)	30/26AWG

If length(meter) is decimal, PN should be as FZU-800-XXM02C,the wire gauge also can be customized.

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by FIBERSTAMP before they become applicable to any particular order or contract. In accordance with the FIBERSTAMP policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
Preliminary	May-13-2025	Advance Release.