53G SFP56 SR Optical Transceiver

FST-50G-SR

Features

- full-duplex transceiver modules
- Transmission data rate up to 53Gbps per channel
- 53Gbps PAM4 transmitter and PAM4 receiver
- 850nm VCSEL array
- PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Power consumption <2W
- Hot Pluggable SFP form factor and Compliant with SFF-8431,SFF-8472
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF with FEC
- Dual LC connector receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

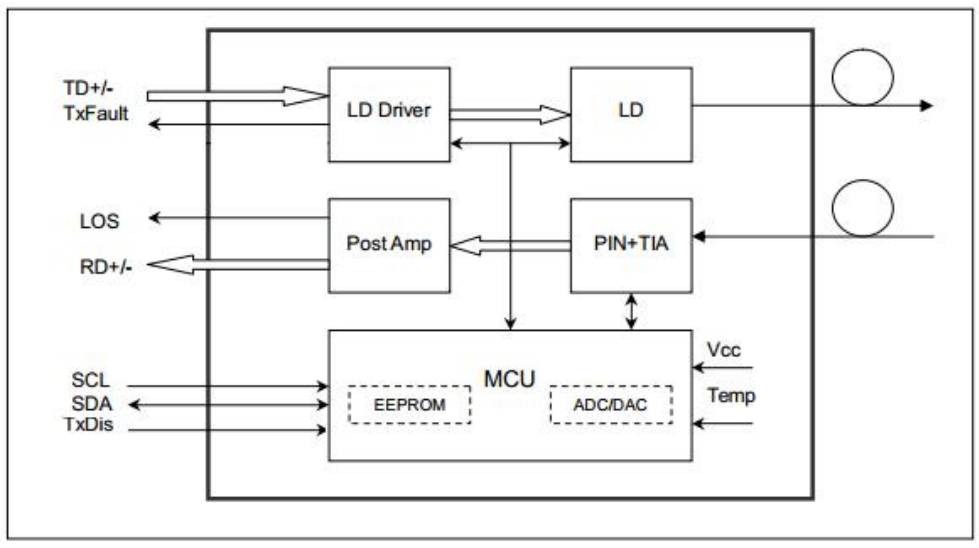
Applications

- IEEE 802.3cd 50GBASE-SR

Description

The FIBERSTAMP Technologies FST-50G-SR is a single-Channel, Pluggable, Fiber-Optic SFP56 for 26.5625GBd PAM4 Ethernet Applications. It is a high performance module for short-range data communication and interconnect applications which operate at 53.125Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 20 contact edge type connector. The optical interface uses duplex LC receptacle. This module incorporates FIBERSTAMP Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit

Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	℃
Data Rate Per Lane	fd		26.5625		GBd
Humidity	Rh	5		85	%
Power Dissipation	Pm			2	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude aAmplitude	ΔVin			900	mVp-p
Differential output voltage amplitude	ΔVout			900	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			2.4E-4	-
Near-end Eye Width at 10^-6 probability(EW6)		0.265			UI
Near-end Eye Height at 10^-6 probability(EH6)		70			mV
Far-end Eye Width at 10^-6 probability(EW6)		0.20			UI
Far-end Eye Height at 10^-6 probability(EH6)		30			mV
Near-end Eye Linearity		0.85			-

Note：

1. BER=2.4E-4; PRBS31Q@26.5625GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.6	nm	-
Average launch power, each lane	Pout	-6	-	4	dBm	-
Optical Modulation Amplitude (OMAouter), each lane	OMA	-4		3	dBm	-
Transmitter and dispersion eye closure(TDEC)	TDEC			4.9	dB	
Extinction Ratio	ER	3	-	-	dB	-
Average launch power of OFF transmitter				-30	dB	-
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Receiver Sensitivity in OMAout	RXsen			-6.5	dBm	1
Stressed Receiver Sensitivity in OMAout				-3.4	dBm	1
Maximum Average power at receiver , each lane input, each lane				4	dBm	-
Minimum Average power at receiver , each lane		-7.9			dBm	
Receiver Reflectance				-12	dB	-
LOS Assert		-10.5			dBm	-
LOS De-Assert – OMA				-10	dBm	-
LOS Hysteresis		0.5			dB	-

Note：

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Per-FEC

Timing and Electrical

Table 4 - Timing and Electrical

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Tx_Disable assert time	t_off		100	µs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		µs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

Diagnostics

Table 5 – Diagnostics Specification

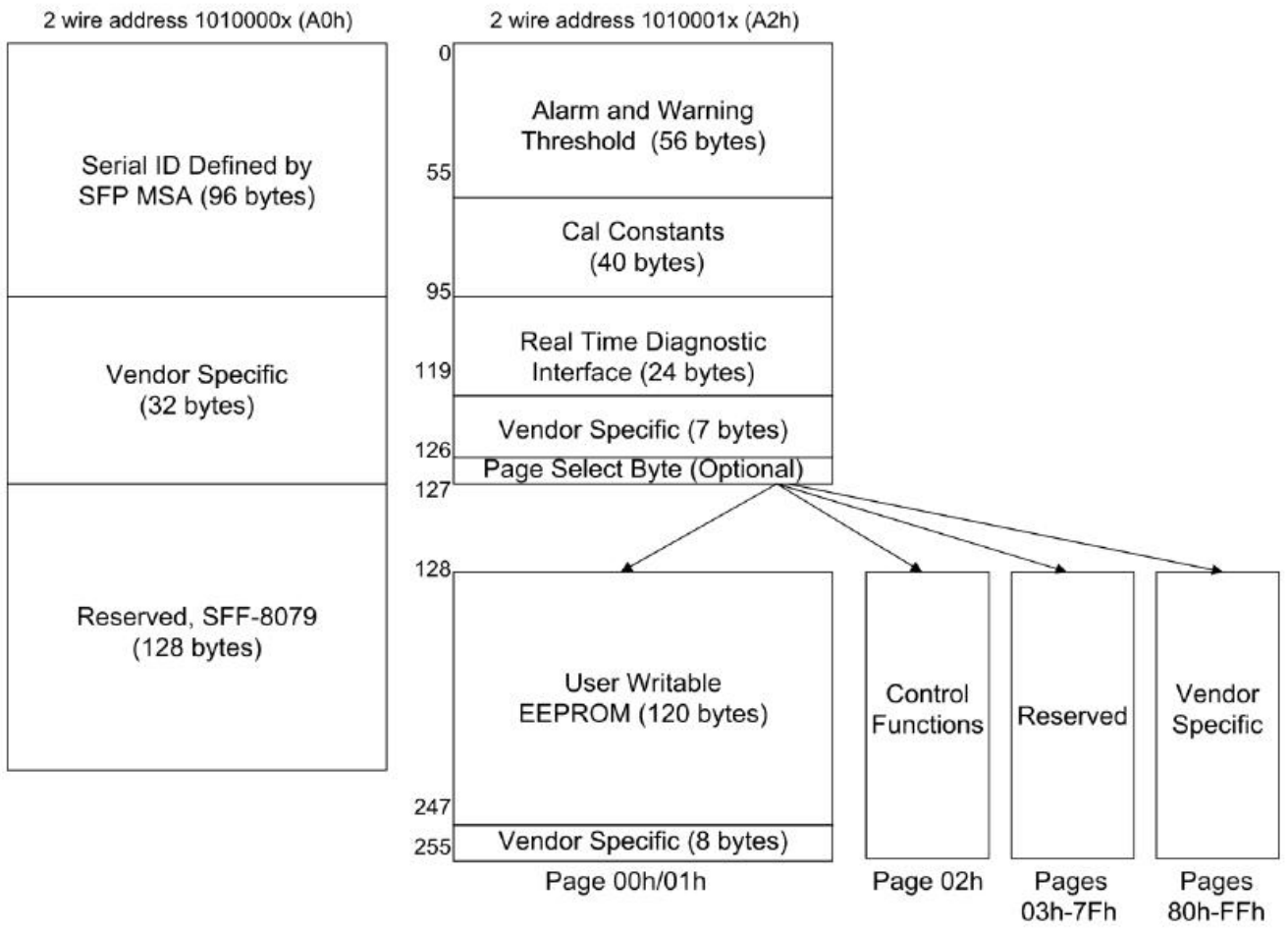
Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to +70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 15	mA	±10%	Internal / External
TX Power	-6 to +4	dBm	±3dB	Internal / External
RX Power	-14 to +4	dBm	±3dB	Internal / External

Digital Diagnostic Memory Map

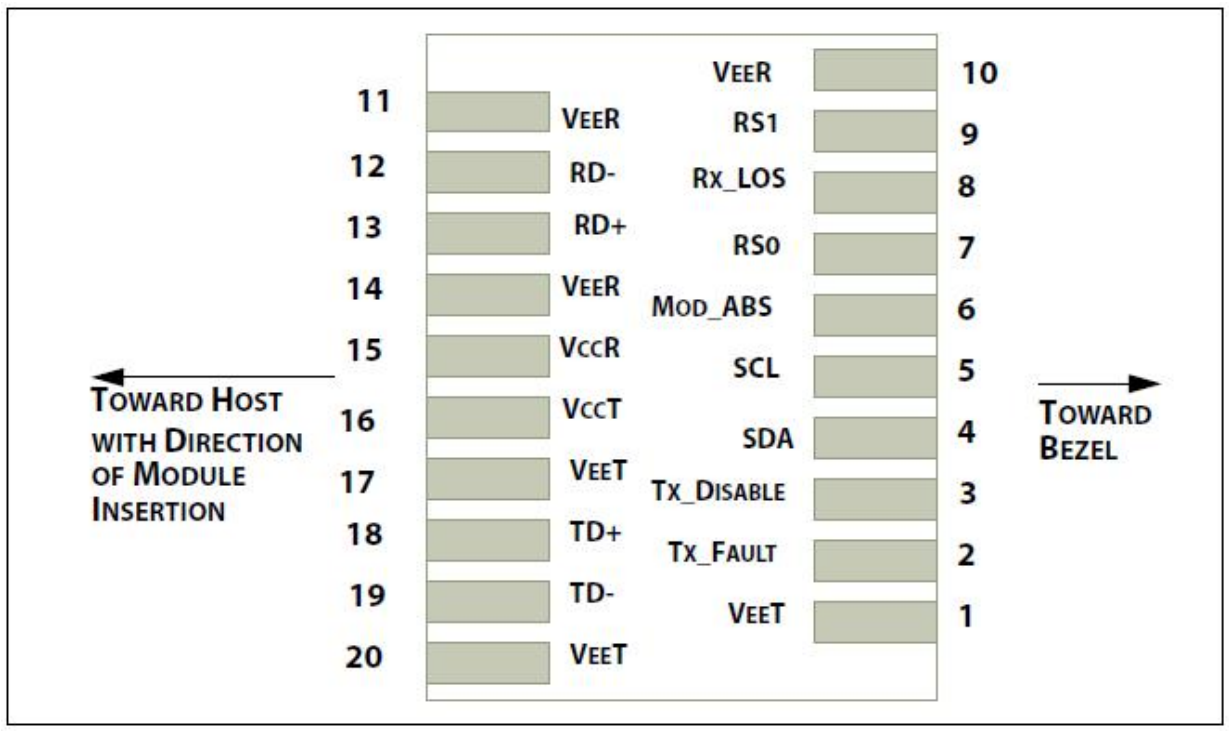
The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

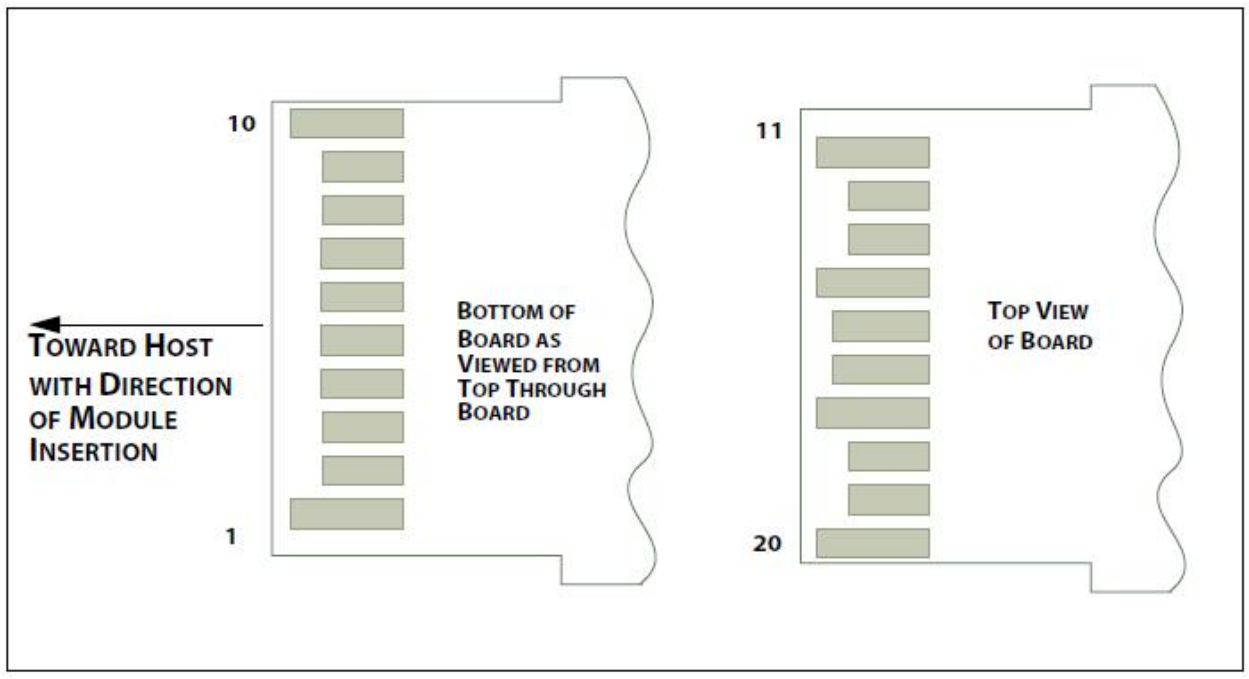
The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following.



Pin Definitions





Pin Descriptions

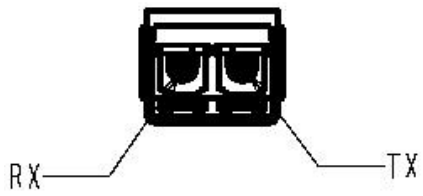
PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

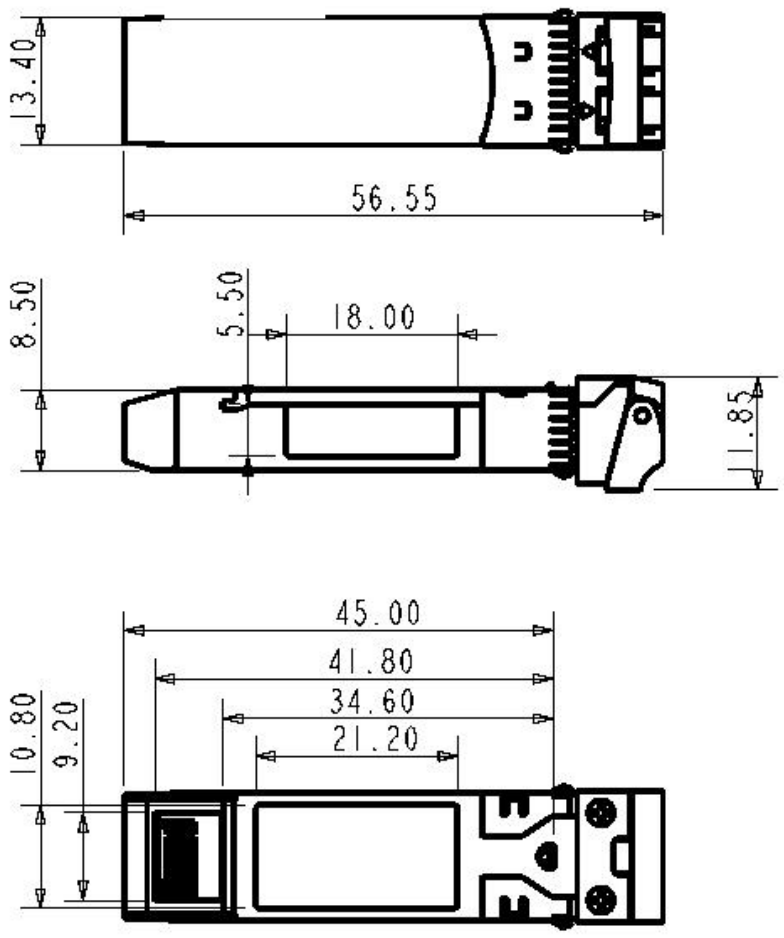
Notes:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Interface Circuit

Mechanical Dimensions





Regulatory Compliance

FIBERSTAMP FST-50G-SR SFP56 transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Laser Eye Safety	TÜV	EN 60825-1:2007 EN 60825-2:2004+A1+A2
Electrical Safety	TÜV	EN 60950
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

References

1. SFP-8472 V12.3
2. SFP-8431
3. IEEE802.3cd 50GBASE-SR
4. OIF CEI-56G-VSR-PAM4

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FST-50G-SR	26.5625GBd PAM4, 850nm, SFP56, OM4,MMF 100m, DDM, 0°C ~ +70°C

Important Notice

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