48Gbps Video QSFP Optical Transceiver, 20km Reach
FHM-3148G-L2CDM

Features

- ✓ 48G-SDI QSFP Transceiver
- ✓ Support for 4 independent 12G/6G/3G/1.5G/270M channels
- ✓ ST 259, ST 292-1,ST 424, ST-2081 and ST-2082 compatible
- ✓ Metal enclosure for Lower EMI
- ✓ 1310nm DFB laser transmitter
- ✓ Each channel can be Supports SDI pathological patterns for SD-SDI, HD-SDI, 3G-SDI,6G-SDI and 12G SDI
- ✓ Compliant with SFF-8436
- ✓ MPO connector
- ✓ The module's receiver contains reclocker
- ✓ ROHS compliant and lead free
- ✓ single 3.3V power supply
- ✓ Hot-pluggable QSFP footprint
- ✓ Operating case temperature range：0 to +70°C

Applications

- ✓ ST 259, ST 292-1, ST 424, ST-2081 and ST-2082 Electrical-to-Optical Interfaces
- ✓ UHDTV/HDTV/SDTV Service Interfaces
- ✓ Live Broadcast and Video Meeting
- ✓ 8K Screen and Camera
- ✓ Security Monitoring

Description

Fiberstamp's GHM-3148G-L2CDM is designed to transmit/receive data rates from 50Mbps to 11.88Gbps，compliant with SMPTE ST 2082-1 (12G UHD-SDI), ST 2081-1 (6G UHD-SDI), ST424 (3G SDI), ST 292-1 (HD-SDI), and ST 259 (SD-SDI). Fiberstamp's Video transceiver supports SDI pathological patterns signals.

The GHM-3148G-L2CDM is packaged in QSFP and supports optical fiber applications up to 20Km.It conforms to the SFF-8436 protocol and can convert bidirectional between SDI and optical fiber at the same time, and different video formats can be used in each transmission direction.Suitable for broadcasting grade HD 12G/6G/3G/HD SDI signal long-distance optical fiber transmission applications.

The transceiver includes threse sections: a DFB laser, a PIN photodiode integrated with a trans-impedance preamplifier (TIA) , Reclocker ,and a MCU controller. The transceiver is compliant with QSFP Multi-Source Agreement (MSA) .

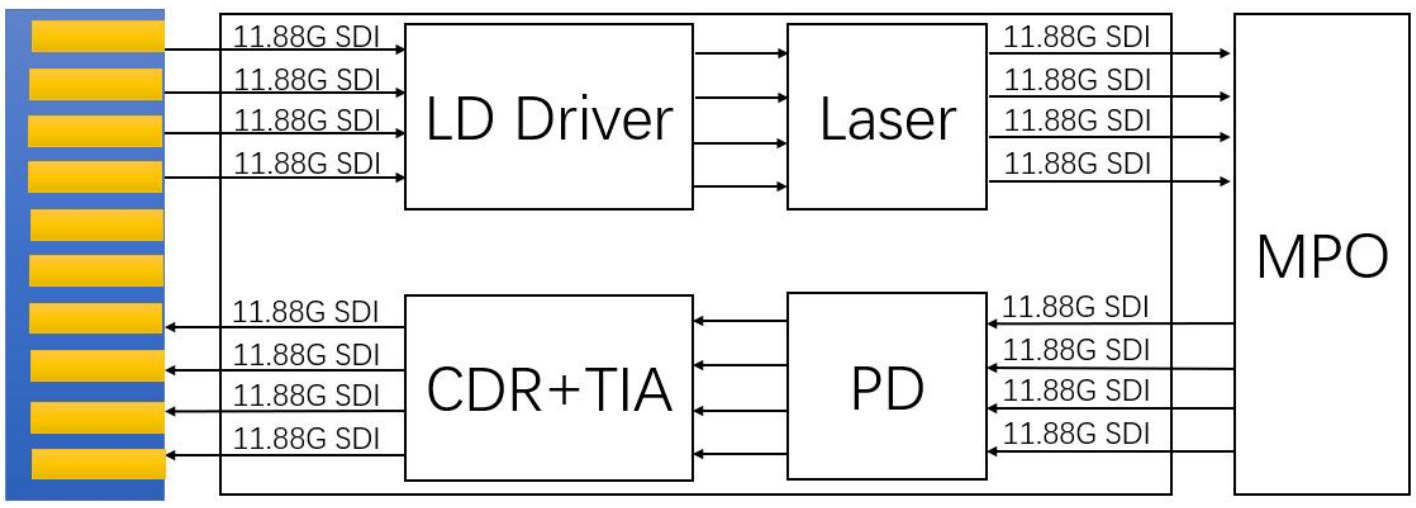

Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	-0.5	4	V
Storage Temperature	T_s	-40	+85	°C

Operating Humidity	-	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case	T_c	0		+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc		1100	1300	mA
Data Rate(each channal)			11.88		Gbps

Optical and Electrical Characteristics

Parameter			Symbol	Min	Typical	Max	Unit	Notes
Transmitter								
Center Wavelength			λc	1300	1310	1320	nm	
Spectral Width (-20dB)			σ			1	nm	
Side Mode Suppression Ratio			SMSR	30			dB	
Average Output Power			Pout	-3		1	dBm	1
Extinction Ratio			ER	3.5			dB	
Data Input Swing Differential			V_{IN}	400		1000	mV	2
Input Differential Impedance			Z_{IN}	90	100	110	Ω	
Rise/Fall Time (20%~80%)		SD-SDI	tr/tf			1500	ps	3
		HD-SDI				270		
		3G-SDI				135		
		6G-SDI				80		
		12G-SDI				45		
Output Jitter	Timing Jitter	SD-SDI				0.2	UI	4
		HD-SDI				1		
		3G-SDI				2		
		6G-SDI				4		
		12G-SDI				8		
	Alignment Jitter	SD-SDI				0.2		
		HD-SDI				0.2		
		3G-SDI				0.3		
		6G-SDI				0.3		
		12G-SDI				0.3		
TX Disable	Disable			2.0		Vcc	V	
	Enable			0		0.8	V	
TX Fault	Fault			2.0		Vcc	V	
	Normal			0		0.8	V	
Receiver								
Center Wavelength			λ_C	1260		1580	nm	
Receiver Sensitivity each lanec (OMA)@ 10.3125G PRBS						-13	dBm	
Receiver Sensitivity each lanec @ 11.88Gbps SDI pathological patterns						-11	dBm	5
Receiver Sensitivity each lanec @ 5.94Gbps SDI pathological patterns						-11	dBm	
Receiver Sensitivity each lanec @ 2.97Gbps SDI pathological patterns						-11	dBm	
Receiver Overload						1	dBm	6
LOS De-Assert			LOS_D			-13	dBm	
LOS Assert			LOS_A	-23			dBm	
LOS Hysteresis			LOS_H	1		4	dB	
Data Output Swing Differential			Vout	400	800	800	mV	3
LOS			High	2.0		Vcc	V	
			Low			0.8	V	

Note:

1. The optical power is launched into SMF.
2. PECL input, internally AC-coupled and terminated.
3. Rise and fall times, 20% to 80%, are measured following a fourth-order Bessel-Thompson filter with a bandwidth of 0.75 x clock frequency corresponding to the serial data rate.
4. UI means one period.
5. Measured with Pathological Patterns 11.88Gpbs(4096*2160 P60,100% Bars);5.94Gpbs (4096*2160 P29.97,100% Bars);2.97Gpbs (2048*1080 P50,100% Bars).
6. Internally AC-coupled, minimum input overload power for SMPTE ST 2081-1, SMPTE ST 2082-1.

Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
Temperature Monitor	0 to +70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 100	mA	±10%	Internal / External
TX Power	-3to +1	dBm	±3dB	Internal / External
RX Power	-20to +1	dBm	±3dB	Internal / External

I2C Bus Interface

The I2C bus interface uses the 2-wire serial CMOS E2PROM protocol. The serial interface meets the following specifications:

1.Support a maximum clock rate of 280Khz.

2. Input/Output levels comply with LVCMOS/LVTTL or compatible logics.

Low: 0 – 0.8 V

High: 2.0 – 3.3 V

Undefined: 0.8 – 2.0 V

Pin Description

Pin	Signal Name	Description	Plug Seq.
1		GND	Module Ground[1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground[1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	MODSEIL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[2]
13		GND	Module Ground[1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[2]
32		GND	Module Ground[1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[1]

Note:

Module circuit ground is isolated from module chassis ground within the module.

Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

Pin Definition

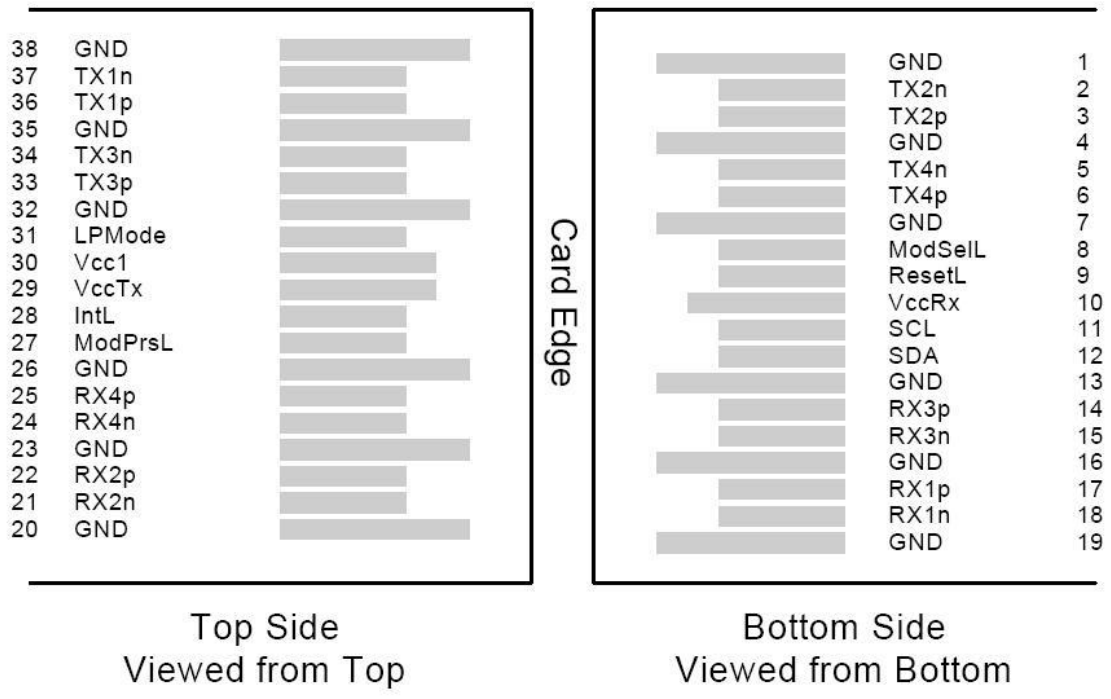

Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Fiberstamp QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low" , it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

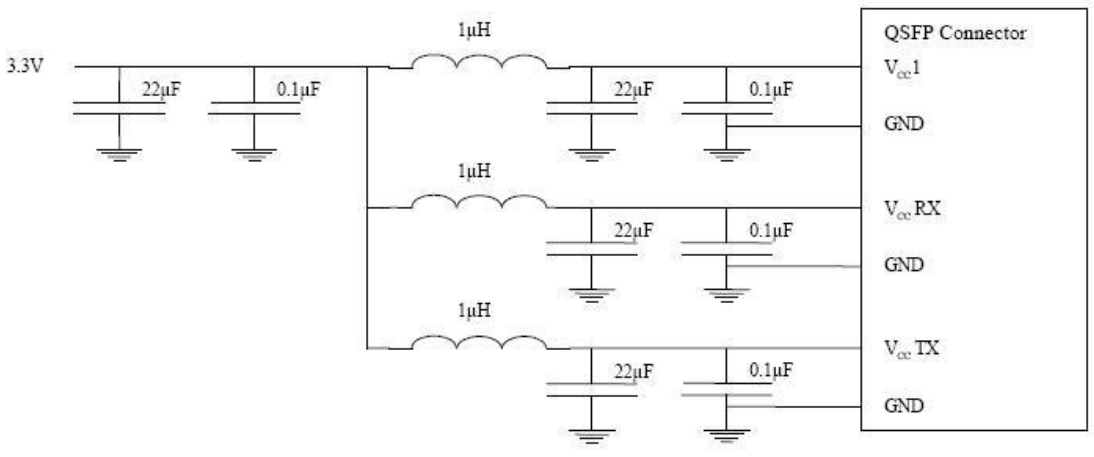

Figure 3. Host Board Power Supply Filtering

Mechanical Dimensions

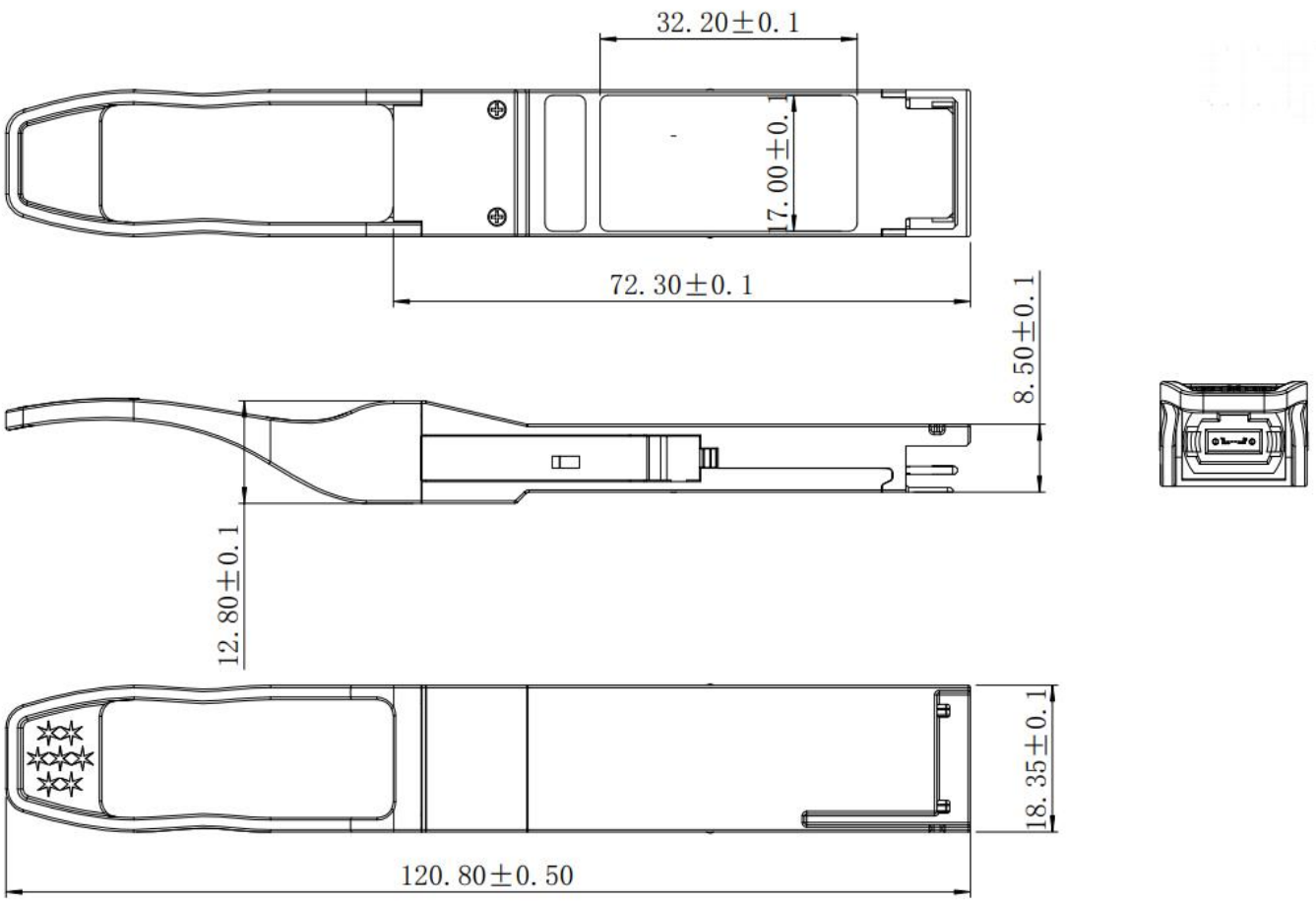

Figure 4. Mechanical Specifications

Regulatory Compliance

Feature	Standard

Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
FHM-3148G-L2CDM	1310nm, 48Gbps, 10/20km,SD/HD/3G/6G/12G SDI Transceiver, MSA

Important Notice

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Revision History

Revision	Date	Description
V0	20-Sep- 2023	Advance Release.