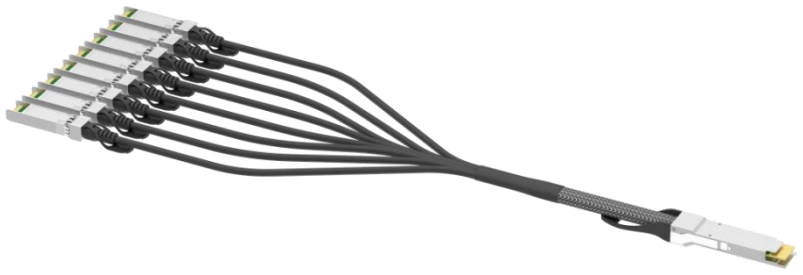
400G QSFP56-DD to 8x50G SFP56 Breakout Passive Direct-Attached Copper Cables

FWL8D-400xxxxxC

Features

- Hot-plug QSFP56-DD and SFP56 form factor
- Support 8x 50Gb/s PAM4 modulation
- Commercial case temperature range of 0℃ to 70℃
- 26 AWG ~30 AWG support up to 3m length max
- I^2C management interface
- RoHS compliant



Applications

- Data storage and communication industry
- Switch / router / HBA
- Enterprise network
- SAN
- Data Center Network

STANDARDS COMPLIANCE

- IEEE802.3cd/802.3bj/802.3by
- QSFP-DD MSA
- SFF-8636

Description

FIBERSTAMP's FWL8D-400xxxxxC cable assembly is used in 8 X 50 Gigabit Ethernet links over copper cable, which provides connectivity between system units with a 400GbE connector on one side and eight separate 50GbE connectors on the other four sides. The cable connects data signals from each of the 16 pairs on the single QSFP56-DD end to the 8 SFP56 multiport ends.

FIBERSTAMP's FWL8D-400xxxxxC cable assemblies is compliant with the QSFP-DD-MSA and IEEE802.3cd/802.3bj/802.3by,it's high performance, cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 400Gigabit Ethernet, Infiniband EDR /HDR and temperature requirements for performance and reliability.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Tc	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	°C
Baud Rate per Lane (PAM4)	fd		26.5625		GBaud/s
Humidity	Rh	5		85	%

Differential Impedance

Parameter	Symbol	Min	Typical	Max	Unit
Differential Impedance(bulk cable)	Rin1,P-P	95	100	110	Ω
Differential Impedance (Mated connector)	Rin2,P-P	90	100	110	Ω
Differential Impedance(cable termination)	Rin3,P-P	85	100	110	Ω

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module GroundNote5
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground Note5
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module GroundNote5
8	LVTTL-I	MODSEIL	Module SelectNote6
9	LVTTL-I	ResetL	Module ResetNote6
10		VCCRx	+3.3V Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clockNote6
12	LVCMOS-I/O	SDA	2-wire Serial interface dataNote6
13		GND	Module GroundNote5
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module GroundNote5
17	CML-O	RX1+	Receiver non-inverted data output

Pin	Logic	Symbol	Name/Description
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module GroundNote5
20		GND	Module GroundNote5
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module GroundNote5
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module GroundNote5
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board2
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power ModeNote6
32		GND	Module GroundNote5
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module GroundNote5
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module GroundNote5
39		GND	Module GroundNote5
40	CML-I	Tx6-	Transmitter inverted data input
41	CML-I	Tx6+	Transmitter non-inverted data input
42		GND	Module Ground Note5
43	CML-I	Tx8-	Transmitter inverted data input
44	CML-I	Tx8+	Transmitter non-inverted data input
45		GND	Module GroundNote5
46		Reserved	
47		TBD	For future use
48		VCC	+3.3V Receiver Power Supply
49		TBD	For future use
50		TBD	For future use
51		GND	Module GroundNote5
52	CML-O	RX7+	Receiver non-inverted data output
53	CML-O	RX7-	Receiver inverted data output

Pin	Logic	Symbol	Name/Description
54		GND	Module GroundNote5
55	CML-O	RX5+	Receiver non-inverted data output
56	CML-O	RX5-	Receiver inverted data output
57		GND	Module GroundNote5
58		GND	Module GroundNote5
59	CML-O	RX6-	Receiver inverted data output
60	CML-O	RX6+	Receiver non-inverted data output
61		GND	Module GroundNote5
62	CML-O	RX8-	Receiver inverted data output
63	CML-O	RX8+	Receiver non-inverted data output
64		GND	Module GroundNote5
65		NC	No connect
66		TBD	For future use
67		VCC	+3.3V Power Supply
68		VCC	+3.3V Power Supply
69		TBD	For future use
70		GND	Module GroundNote5
71	CML-I	Tx7+	Transmitter non-inverted data input
72	CML-I	Tx7-	Transmitter inverted data input
73		GND	Module GroundNote5
74	CML-I	Tx5+	Transmitter non-inverted data input
75	CML-I	Tx5-	Transmitter inverted data input
76		GND	Module GroundNote5

Note :

Note5. Module circuit ground is isolated from module chassis ground within the module.

Note6. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

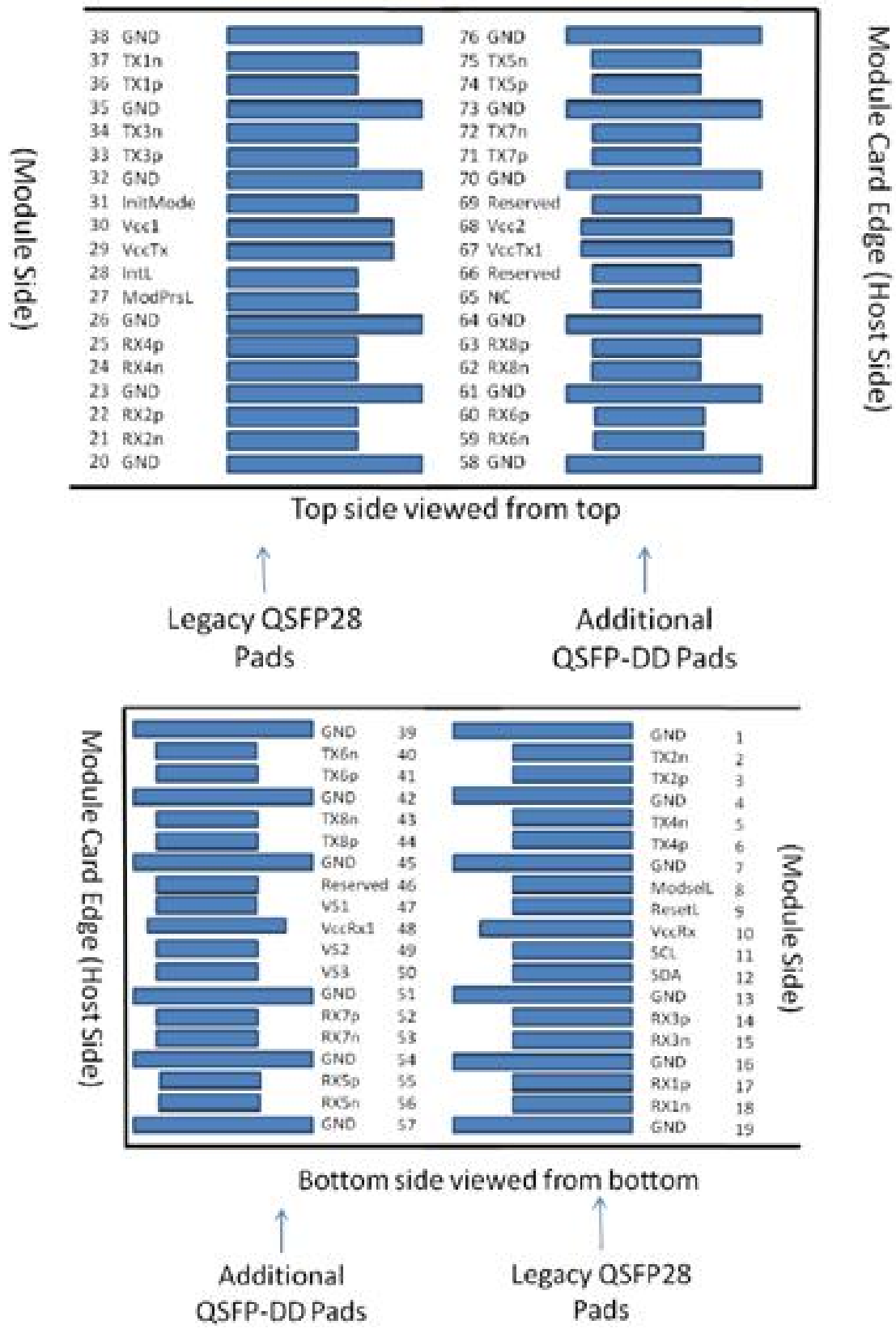


Figure 1. Electrical Pin-out Details

SIGNAL INTEGRITY

A	Time domain parameter	Test condition	Spec		Equipment
1	Differential Impedance(bulk cable)	Tr:25ps	100+10/-5 ohms		E5071C
2	Differential Impedance (Mated connector)		100+/-10 ohms		
3	Differential Impedance(cable termination)		100+10/-15 ohms		
4	Intra-skew		L*15+20	L：length(m)	
				SPEC：ps	
B	**Frequency domain parameter**	**Test condition**	**Test spec(dB)**	**f(GHz)**	
1	SDD11/SD D22	Freq:50MHz ～20GHz Points:1601	-22+20/25.78*f*10^(-3)	0.05≤f<4.1	E5071C
			-10.66+14*log((f*10^(-3))/5.5) ≤5.3dB@13.26GHz	4.1≤f≤19	

2	SCC11/SC C22	Freq:50MHz ～20GHz Points:1601	≤-2dB	0.2≤f≤19	
3	SDC11/SD C22	Freq:50MHz ～20GHz Points:1601	-16+2*f/3	0.05≤f≤2	
5	SCD21- SDD21	Freq:50MHz ～20GHz Points:1601	10　as 0.01≤f < 12.89 -27+29/22*f*0.001　as 12.89≤f < 15.7 6.3 as 15.7≤f≤19	0.01≤f≤19	
6	MDNEXT	Freq:50MHz ～20GHz Points:1601	≤-26dB@12.89GHz	0.01≤f≤19	
7	SDD21	Freq:50MHz ～20GHz Points:1601 IF：1KHz	-0.7*(f*10^(-3))^0.5-0.3*(f*10^(-3))-0.01*(f*10^(-3))^2 <17.16dB@13.26GHz	0.01≤f≤19	
8	COM	IEEE802.3cd	>3dB		

Mechanical Dimensions

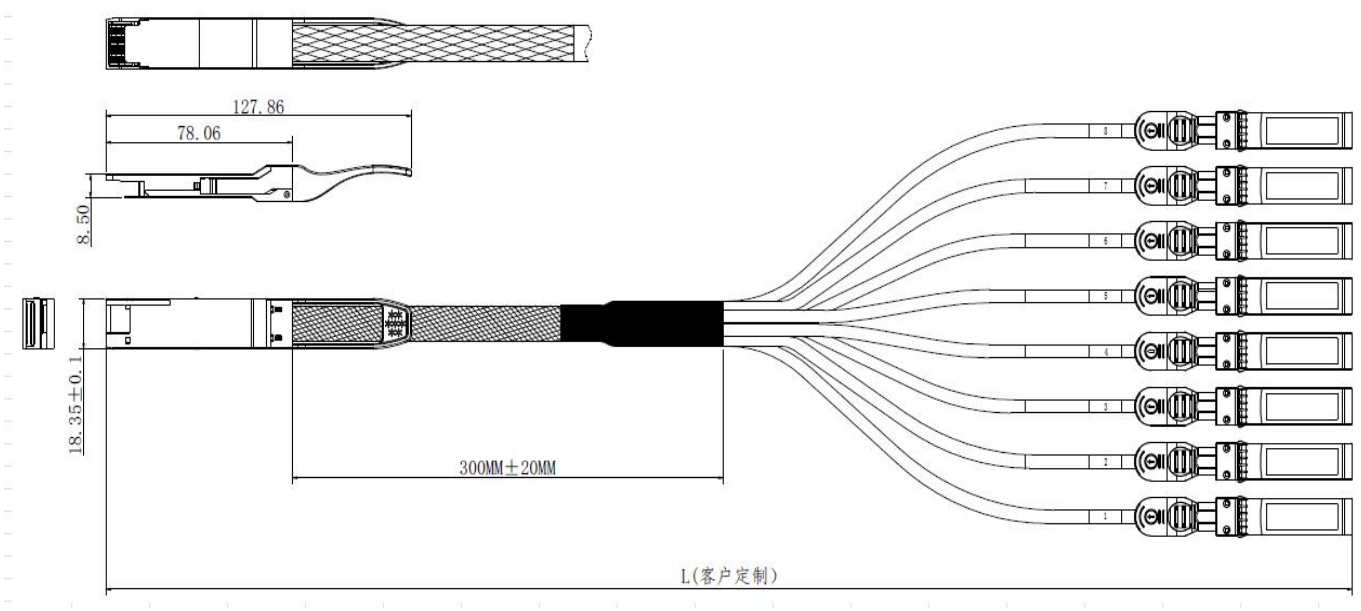
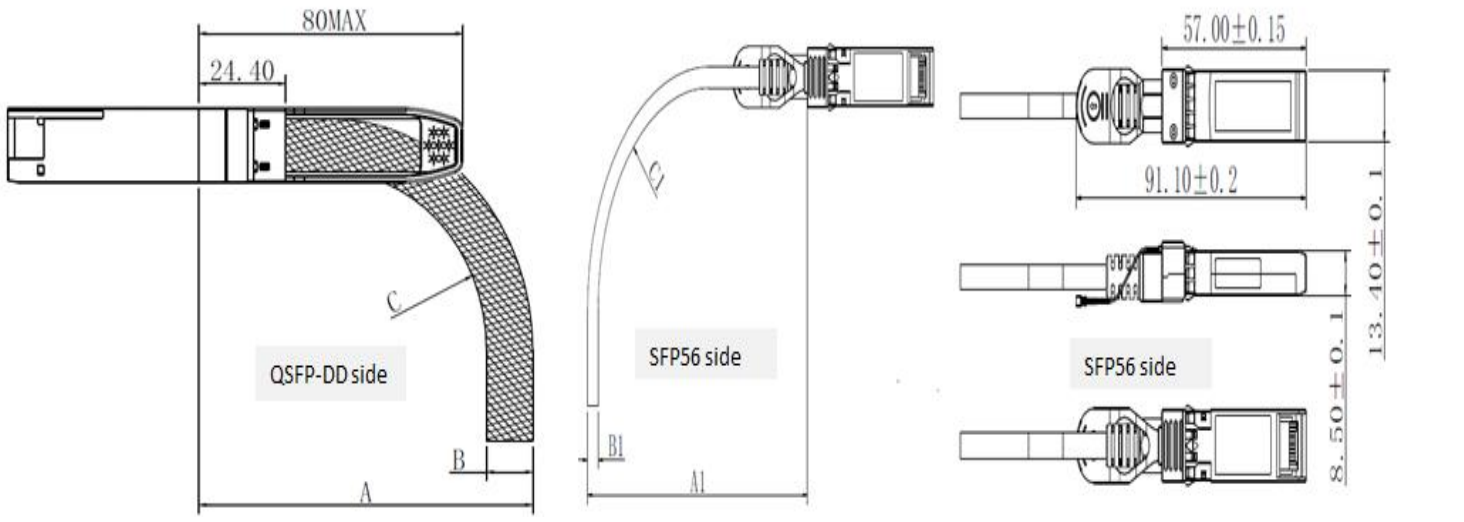


Figure 2. Typical mechanical structure



QSFP DD				SFP56			
CABLE GUAGE	DIAMETER"B"	MIN. BEND RADIUS"C"	MIN. BEND RADIUS"A"	CABLE GUAGE	DIAMETER"B1"	MIN. BEND RADIUS"C1"	MIN. BEND RADIUS"A1"
26AWG	11MM	55MM	110MM	26AWG	4.8MM	24MM	65MM

Figure 3. Typical diameter and bend radius

Wiring connection diagram

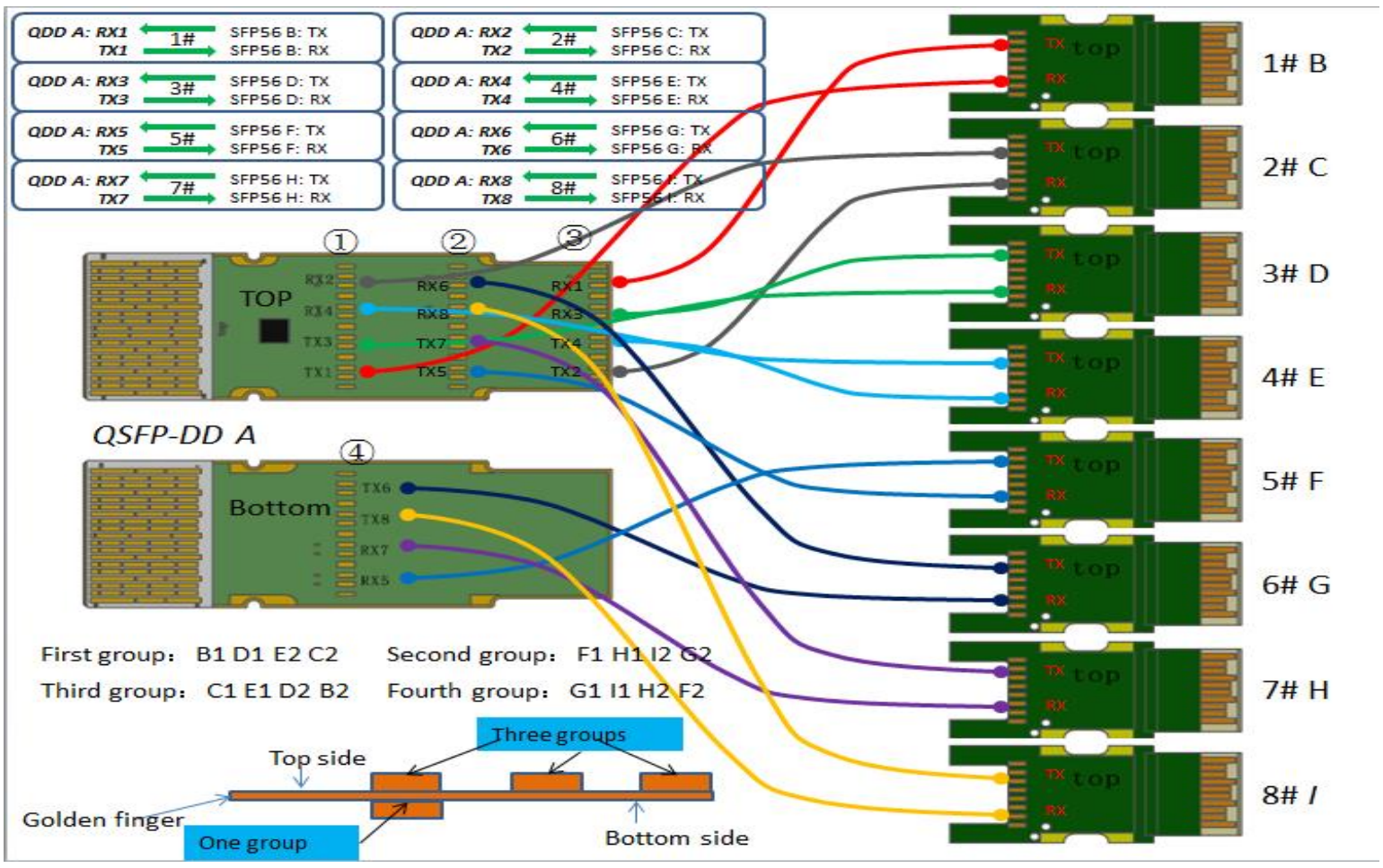


Figure 4. Wiring connection diagram

Regulatory Compliance

FIBERSTAMP FWL8D-400xxxxxC passive cable assemblies meet the requirements of the following standards:

Feature	Standard
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

Ordering information

Part Number	FWL8D-400xxxxxC		
Cable Length（meter）	1	2	3
Cable Wire gauge（AWG）	30/26	30/26	26
The cable length and wire gauge can be customized, further details are available from any FIBERSTAMP sales representative.			

Important Notice

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