400G QSFP56-DD to 4x100G QSFP56 Breakout Passive Direct-Attached Copper Cables

FWL4H-400xxxxxC

Features

- Hot-plug QSFP56-DD and QSFP56 form factor
- Support 8x 50Gb/s PAM4 modulation
- Commercial case temperature range of 0℃ to 70℃
- 26 AWG ~30 AWG support up to 3m length
- I^2C management interface
- RoHS compliant

Applications

- Data storage and communication industry
- Switch / router / HBA
- Enterprise network
- SAN
- Data Center Network

STANDARDS COMPLIANCE

- IEEE802.3cd
- QSFP-DD MSA

Description

FIBERSTAMP's FWL4H-400xxxxxCcable assembly is used in 4 X 100 Gigabit Ethernet links over copper cable, which provides connectivity between system units with a 400GbE connector on one side and four separate 100GbE connectors on the other four sides. The cable connects data signals from each of the 16 pairs on the single QSFP56-DD end to the dual pairs of each of the QSFP56 multiport ends.

FIBERSTAMP's FWL4H-400xxxxxCcable assemblies is compliant with the QSFP-DD-MSA and IEEE802.3cd ,it's high performance, cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 400Gigabit Ethernet, InfiniBand EDR /HDR and temperature requirements for performance and reliability.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-20	85	℃
Case Operating Temperature	Tc	0	70	℃
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	℃
Baud Rate per Lane (PAM4)	fd		26.5625		GBaud/s
Humidity	Rh	5		85	%

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[Note5]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground [Note5]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[Note5]
8	LVTTL-I	MODSEIL	Module Select[Note6]
9	LVTTL-I	ResetL	Module Reset[Note6]
10		VCCRx	+3.3V Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[Note6]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[Note6]
13		GND	Module Ground[Note5]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[Note5]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[Note5]
20		GND	Module Ground[Note5]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[Note5]

Pin	Logic	Symbol	Name/Description
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[Note5]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[Note6]
32		GND	Module Ground[Note5]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[Note5]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[Note5]
39		GND	Module Ground[Note5]
40	CML-I	Tx6-	Transmitter inverted data input
41	CML-I	Tx6+	Transmitter non-inverted data input
42		GND	Module Ground [Note5]
43	CML-I	Tx8-	Transmitter inverted data input
44	CML-I	Tx8+	Transmitter non-inverted data input
45		GND	Module Ground[Note5]
46		Reserved	
47		TBD	For future use
48		VCC	+3.3V Receiver Power Supply
49		TBD	For future use
50		TBD	For future use
51		GND	Module Ground[Note5]
52	CML-O	RX7+	Receiver non-inverted data output
53	CML-O	RX7-	Receiver inverted data output
54		GND	Module Ground[Note5]
55	CML-O	RX5+	Receiver non-inverted data output
56	CML-O	RX5-	Receiver inverted data output
57		GND	Module Ground[Note5]
58		GND	Module Ground[Note5]
59	CML-O	RX6-	Receiver inverted data output

Pin	Logic	Symbol	Name/Description
60	CML-O	RX6+	Receiver non-inverted data output
61		GND	Module Ground[Note5]
62	CML-O	RX8-	Receiver inverted data output
63	CML-O	RX8+	Receiver non-inverted data output
64		GND	Module Ground[Note5]
65		NC	No connect
66		TBD	For future use
67		VCC	+3.3V Power Supply
68		VCC	+3.3V Power Supply
69		TBD	For future use
70		GND	Module Ground[Note5]
71	CML-I	Tx7+	Transmitter non-inverted data input
72	CML-I	Tx7-	Transmitter inverted data input
73		GND	Module Ground[Note5]
74	CML-I	Tx5+	Transmitter non-inverted data input
75	CML-I	Tx5-	Transmitter inverted data input
76		GND	Module Ground[Note5]

Note:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

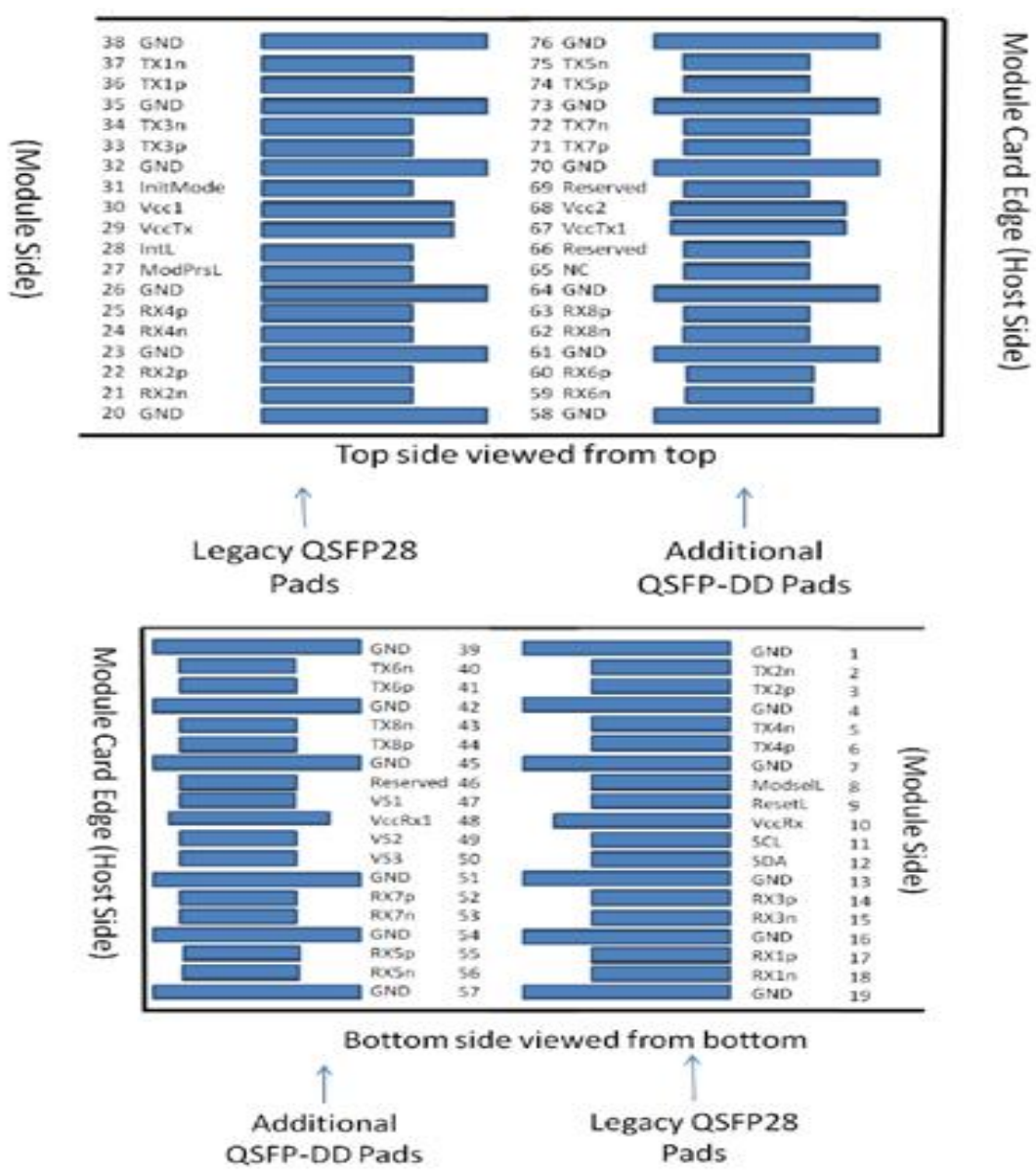

Figure 1. Electrical Pin-out Details

SIGNAL INTEGRITY

A	Time domain parameter	Test condition	SPEC		Equipment
1	Differential Impedance(bulk cable)	TDR Tr:25ps	100+10/-5 ohms		E5071C
2	Differential Impedance (Mated connector)		100+/-10 ohms		
3	Differential Impedance(cable termination)		100+10/-15 ohms		
4	Intra-skew		L*15+20	L:length(m) SPEC:ps	
B	**Frequency domain parameter**	**Test condition**	**Test spec(dB)**	**f(GHz)**	**Equipment**
1	SDD11/SDD22	Freq:50MHz～20GHz Points:1601	-22+20/25.78*f*10^(-3) -10.66+14*log((f*10^(-3))/5.5) ≤5.3dB@13.26GHz	0.05≤f<4.1 4.1≤f≤19	E5071C
2	SCC11/SCC22	Freq:50MHz～20GHz Points:1601	≤-2dB	0.2≤f≤19	
3	SDC11/SDC22	Freq:50MHz～20GHz Points:1601	-16+2*f/3	0.05≤f≤2	
4	SCD21- SDD21	Freq:50MHz～20GHz Points:1601	10 as 0.01≤f < 12.89; -27+29/22*f*0.001 as 12.89≤f < 15.7; 6.3 as 15.7≤f≤19	0.01≤f≤19	
5	MDNEXT	Freq:50MHz～20GHz Points:1601	≤-26dB@12.89GHz	0.01≤f≤19	
6	SDD21	Freq:50MHz～20GHz Points:1601 IF: 1KHz	0.7*(f*10^(-3))^0.5-0.3*(f*10^(-3)) -0.01*(f*10^(-3))^2 <17.16dB@13.26GHz	0.01≤f≤19	
7	COM	IEEE802.3cd	>3dB		

Mechanical Dimensions

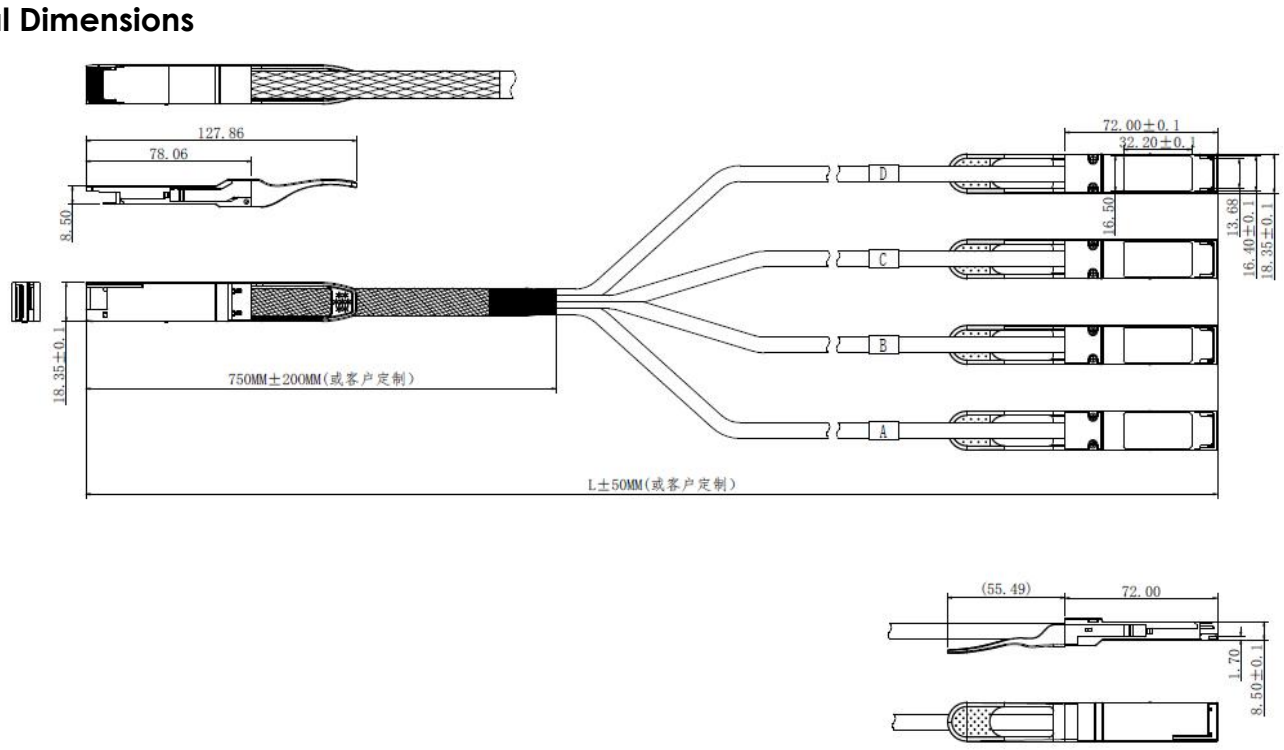

Figure 2. Mechanical Specifications

Wiring Patterns

P1, QSFP56-DD			P2, QSFP56	
GND			GND	
TX1+	36		17	RX1+
TX1−	37		18	RX1−
TX2+	3		22	RX2+
TX2−	2		21	RX2−
RX1+	17		36	TX1+
RX1−	18		37	TX1−
RX2+	22		3	TX2+
RX2−	21		2	TX2−
GND			GND	

P1, QSFP56-DD			P4, QSFP56	
GND			GND	
TX5+	74		17	RX1+
TX5−	75		18	RX1−
TX6+	41		22	RX2+
TX6−	40		21	RX2−
RX5+	55		36	TX1+
RX5−	56		37	TX1−
RX6+	60		3	TX2+
RX6−	59		2	TX2−
GND			GND	

P1, QSFP56-DD			P3, QSFP56	
GND			GND	
TX3+	33		17	RX1+
TX3−	34		18	RX1−
TX4+	6		22	RX2+
TX4−	5		21	RX2−
RX3+	14		36	TX1+
RX3−	15		37	TX1−
RX4+	25		3	TX2+
RX4−	24		2	TX2−
GND			GND	

P1, QSFP56-DD			P5, QSFP56	
GND			GND	
TX7+	71		17	RX1+
TX7−	72		18	RX1−
TX8+	44		22	RX2+
TX8−	43		21	RX2−
RX7+	52		36	TX1+
RX7−	53		37	TX1−
RX8+	63		3	TX2+
RX8−	62		2	TX2−
GND			GND	

Figure 3. Wiring Patterns

Wiring connection diagram

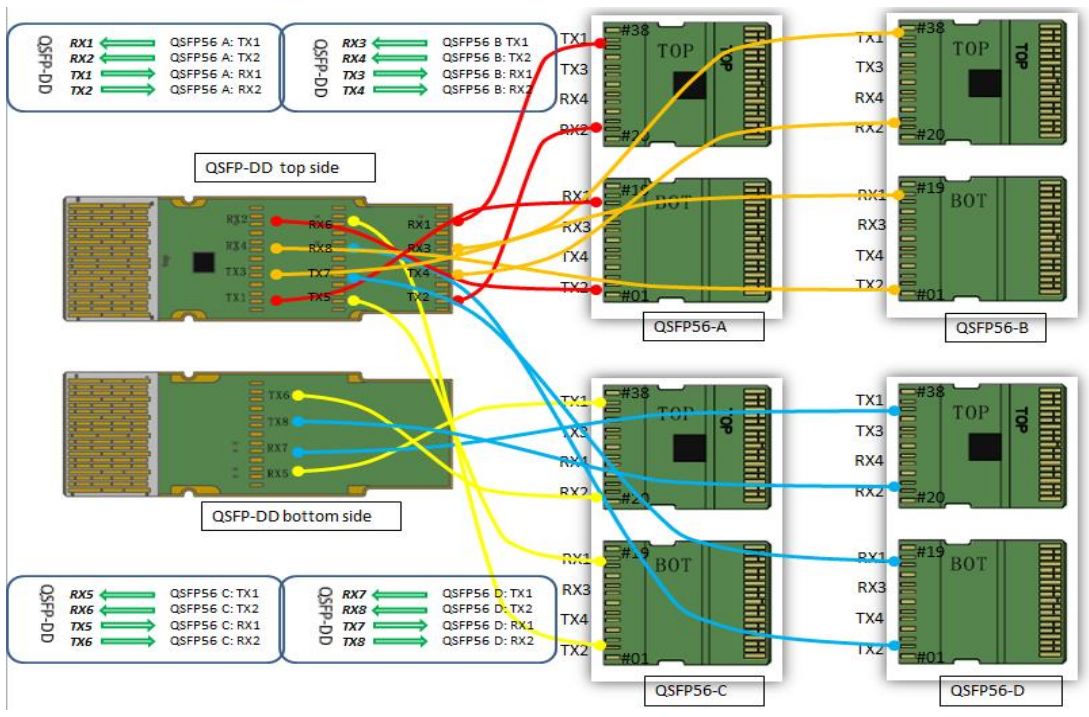

Figure 4. Wiring connection diagram

Regulatory Compliance

FIBERSTAMP FWL4H-400xxxxxCpassive cable assemblies meet the requirements of the following standards:

Feature	Standard
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

Ordering information

Part Number	FSDB4D-400G-xM		
Length (meter)	1	2	3
Wire gauge (AWG)	30/26	30/26	26

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by FIBERSTAMP before they become applicable to any particular order or contract. In accordance with the FIBERSTAMP policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of FIBERSTAMP or others. Further details are available from any FIBERSTAMP sales representative.

www.fiberstamp.com
sales@fiberstamp.com
FIBERSTAMP Co,.Ltd.