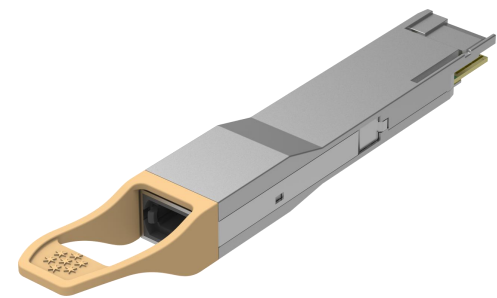


400G QSFP-DD SR8 850nm 100m Optical Transceiver Module

Features

- Hot-pluggable QSFP-DD form factor
- 8 channels full-duplex transceiver module
- 8x 850nm VCSEL array and PIN photo-detector array
- Internal DSP CDR circuits on both receiver and transmitter channels
- Compliant with QSFP-DD MSA, CMIS and IEEE 802.3cd 200GBASE-SR4
- Data rate up to 425Gbps (8x 50G PAM4)
- Reach up to 70m (OM3) or 100m (OM4) over MMF with FEC
- Power consumption < 10W
- MPO24 receptacle
- Built-in digital diagnostic functions
- Operating case temperature range from 0°C to 70°C
- 3.3V power supply voltage
- RoHS compliant (lead free)



Applications

- IEEE 802.3cd 200GBASE-SR4

Description

The FiberStamp 400G QSFP-DD SR8 optical transceiver is designed for Data Center 2x 200GBASE-SR4 Ethernet links. It integrates eight data lanes in each direction with 8x 26.5625GBd. Each lane can operate at 53.125Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber with FEC. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 contact edge type connector. The optical interface uses a MTP24/MPO24 PC connector (or MPO16/MTP16 APC connector). The Common Management Interface Specification (CMIS) for QSFP-DD modules, This module incorporates FiberStamp proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

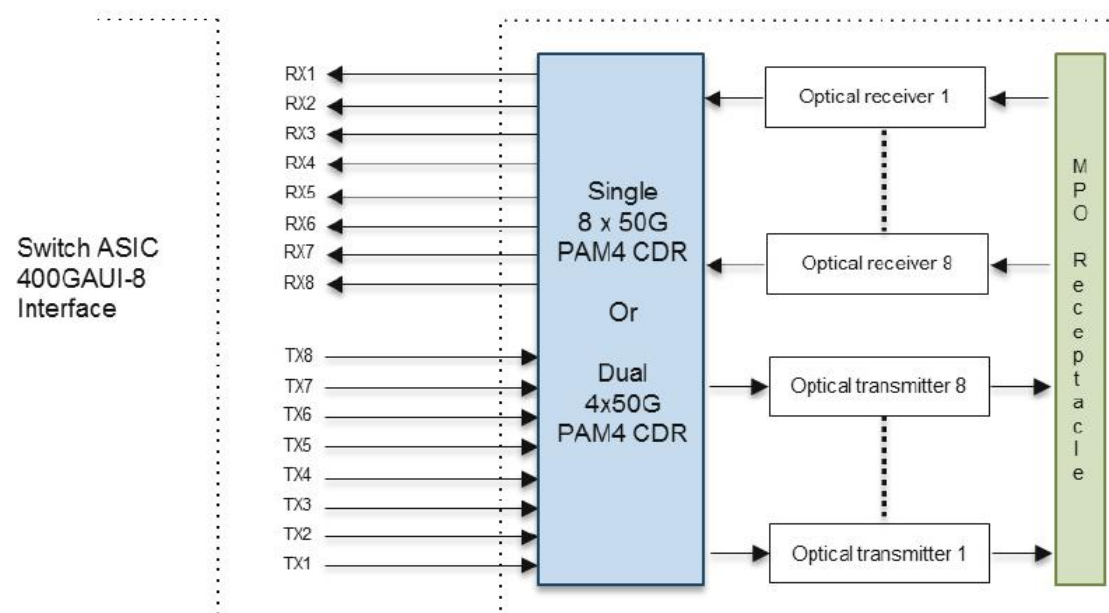


Figure 1. Module Block Diagram



2x200GBASE-SR4 QSFP-DD is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane	fd		26.5625		GBd
Humidity	Rh	5		85	%
Power Dissipation	Pm			10	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin			900	mVp-p
Differential output voltage amplitude	ΔVout			900	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			2.4E-4	-
Near-end Eye Width at 10 ⁻⁶ probability(EW6)		0.265			UI
Near-end Eye Height at 10 ⁻⁶ probability(EH6)		70			mV
Far-end Eye Width at 10 ⁻⁶ probability(EW6)		0.20			UI
Far-end Eye Height at 10 ⁻⁶ probability(EH6)		30			mV
Near-end Eye Linearity		0.85			-

Notes:

1. BER=2.4E-4; PRBS31Q@26.5625GBd. Pre-FEC.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.



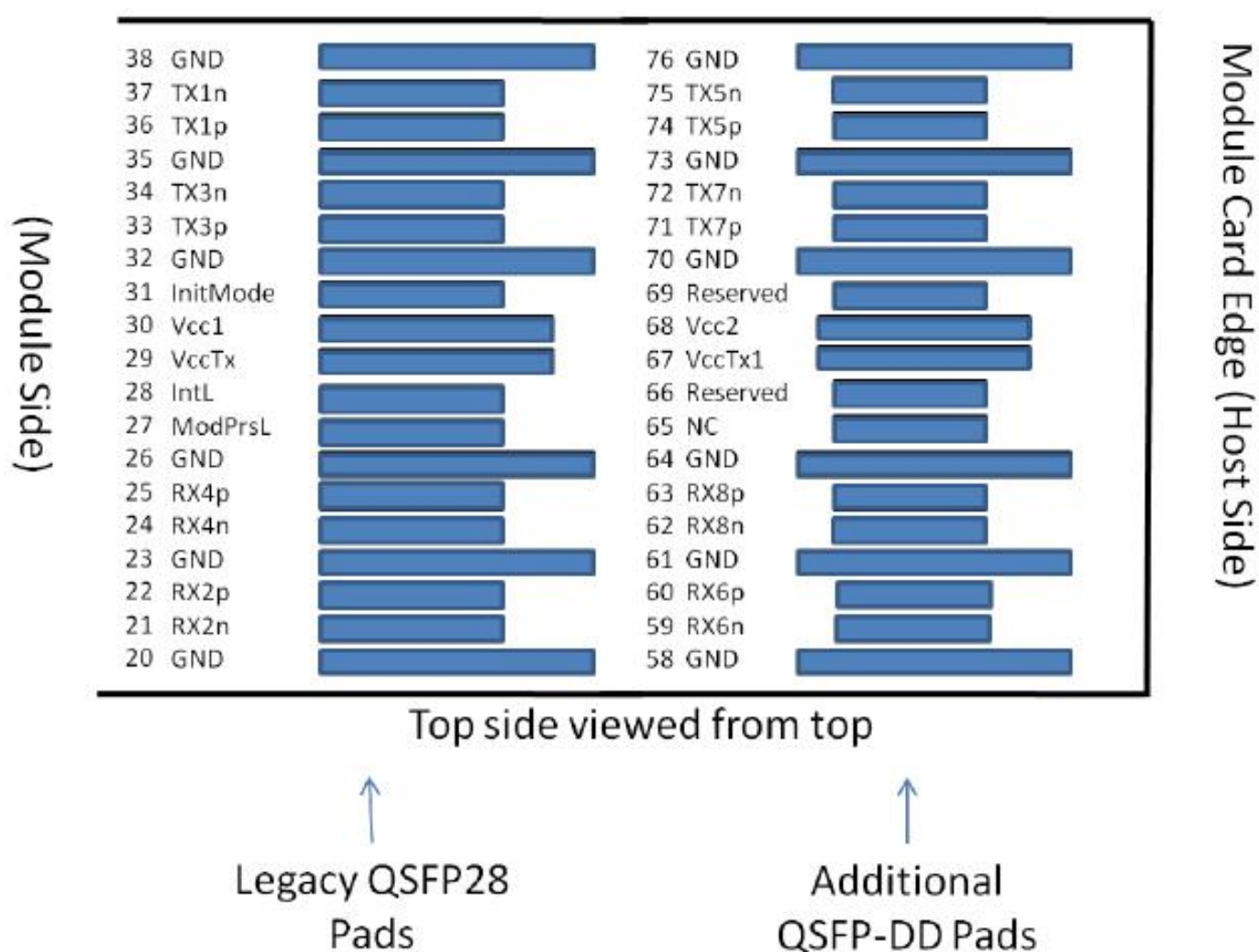
Optical Characteristics

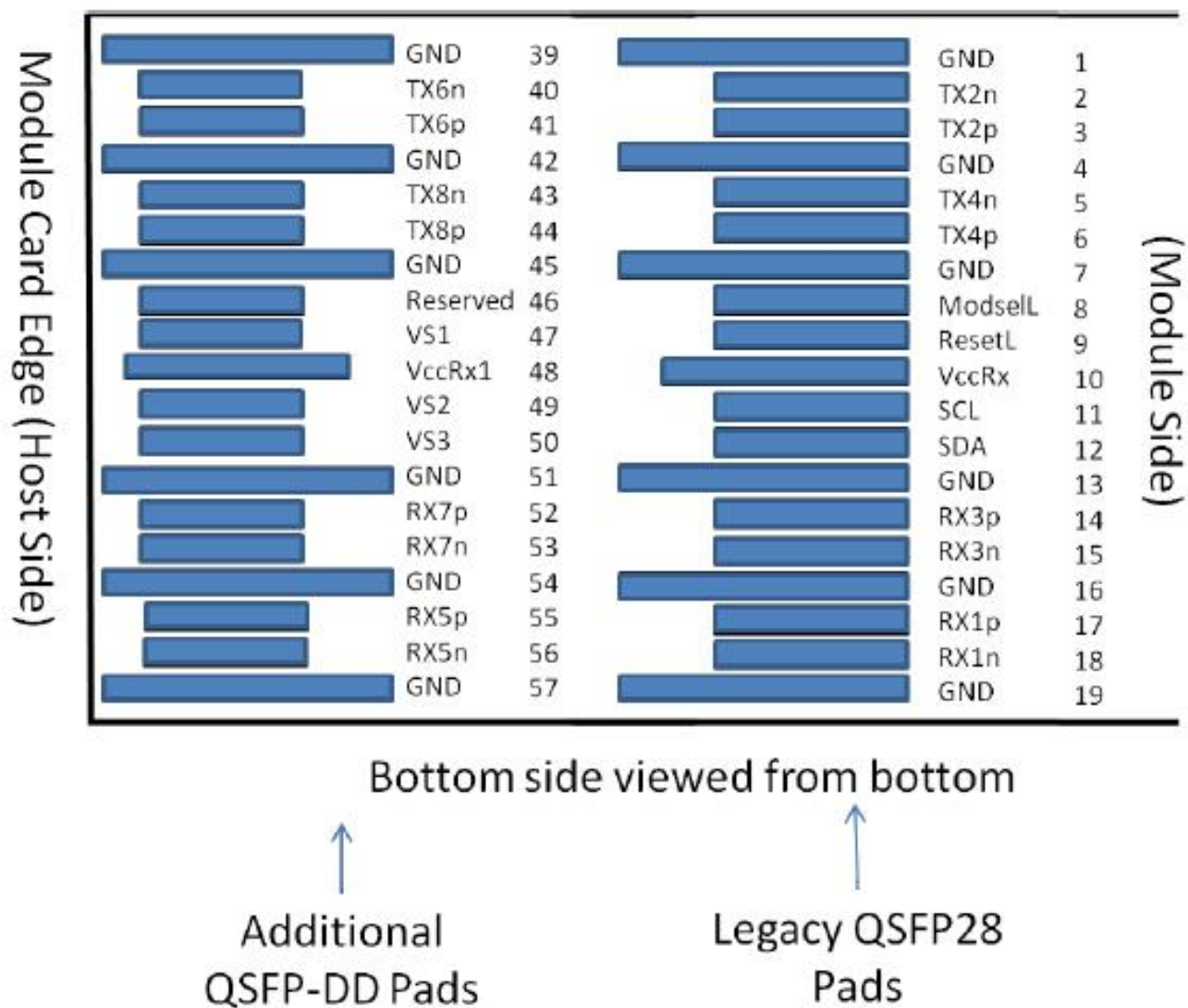
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength	λ_c	840	850	860	nm	-
RMS spectral width	$\Delta\lambda$	-	-	0.6	nm	-
Average launch power, each lane	P _{out}	-6.5	-	4	dBm	-
OMA _{outer} , each lane	OMA	-4.5	-	3	dBm	-
TDEC, each lane	TDEC	-	-	4.5	dB	-
Extinction Ratio	ER	3	-	-	dB	-
Average launch power of OFF, each lane				-30	dB	-
Receiver						
Center Wavelength	λ_c	840	850	860	nm	-
Receiver Sensitivity in OMA _{out}	RX _{sen}	-6.5	-	-3.4	dBm	1
Stressed Receiver Sensitivity in OMA _{out}				-3	dBm	1
Average power input, each lane		-7.9	-	4	dBm	-
Receiver Reflectance				-12	dB	-
LOS Assert		-10			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

Notes:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Pin Description





Bottom side viewed from bottom

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Figure 2. Electrical Pin-out Details



ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_{Reset_init}) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMODE. See SFF-8679 for signal description.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

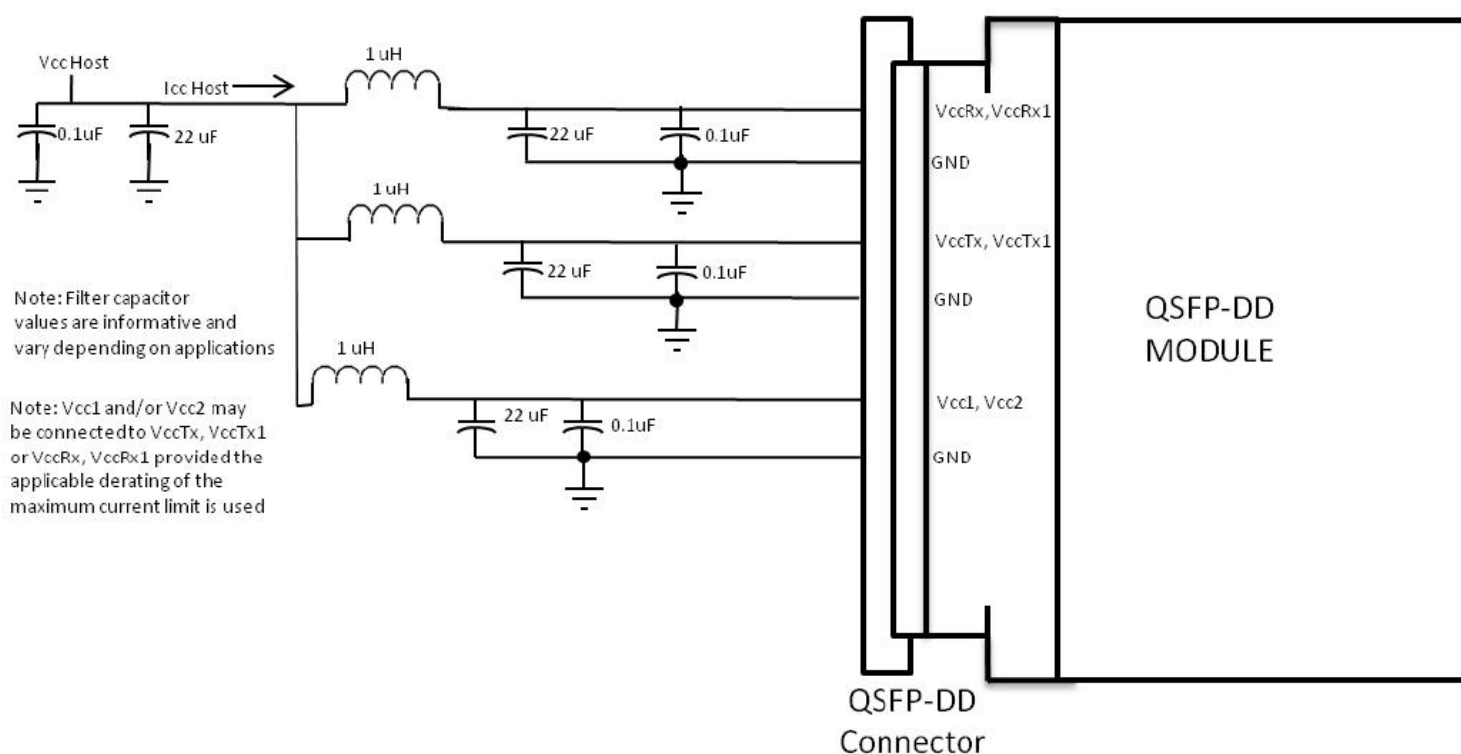
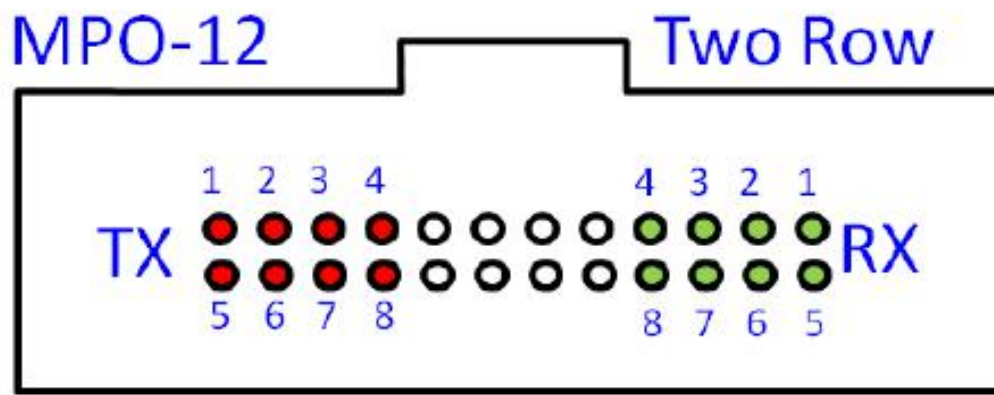


Figure 3. Host Board Power Supply Filtering



Optical Interface Lanes and Assignment

The optical interface port is a male MPO24(MTP24) PC connector for FST-400G-SR8-A.



The optical interface port is a male MPO16(MTP16) APC connector for FST-400G-SR8-B.

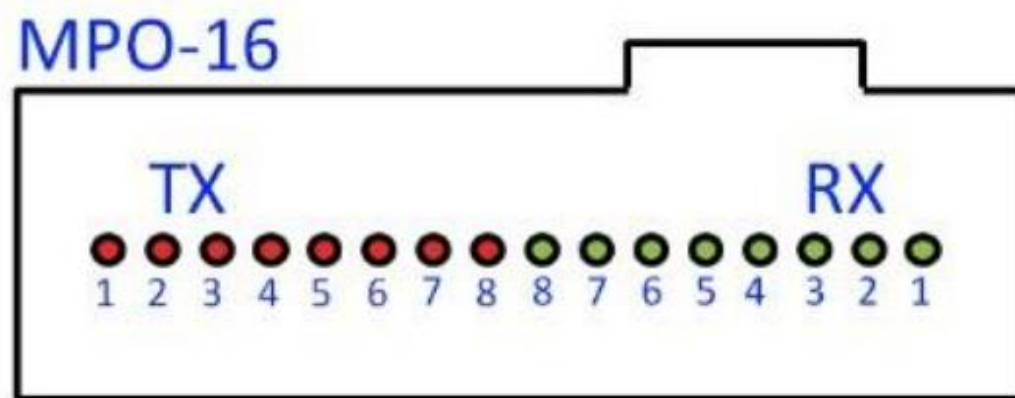


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FiberStamp QSFP-DD products. A 2-wire serial interface provides user to contact with module.

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital 3 monitoring and certain control functions. The interface is mandatory for all CMIS 4 devices. The interface has been designed largely after the QSFP memory map. The memory 5 map has been changed in order to accommodate 8 electrical lanes and limit the required 6 memory space. The single address approach is used as found in QSFP. Paging is used in 7 order to enable time critical interactions between host and module.

The structure of the memory is shown in Figure 5 . The memory space is arranged into a 10 lower, single page, address space of 128 bytes and multiple upper address space pages. 11 This structure supports a flat 256 byte memory for passive copper cables and permits 12 timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical 13 entries, e.g. serial ID information and threshold settings, are available with the Page 14 Select function. The structure also provides address expansion by adding additional upper 15 pages as needed. Upper pages 00-02 all contain static, non-volatile advertising 16 registers. Upper page 01 provides revision codes and advertising registers that indicate 17 the capabilities of the module. Upper page 02 provides thresholds for monitored 18 functions. Upper page 03 provides a user read/write space. The lower page and upper page 19 00 are required for passive copper cables and are always implemented. In addition, upper 20 pages 1, 2 and bank 0 pages 10h and 11h are required for active modules. See CMIS Document Table 40 for 21 details regarding the implementation of optional upper pages and the bank pages. Bank 22 pages are provided to provide the ability to support modules with more than 8 lanes. Bank 23 0 provides lane-specific registers for the lower 8 lanes. Each additional bank provides 24 support for an additional 8 lanes. Reserved bytes are for future use and shall not be 25 used and shall be set to 0. Other organizations shall contact the managing organization 26 or the editor of this document to request allocations of registers. The use of custom 27 bytes is not restricted and may be vendor defined. The use of registers defined as custom 28 may be subject to additional agreements between module users and vendors.



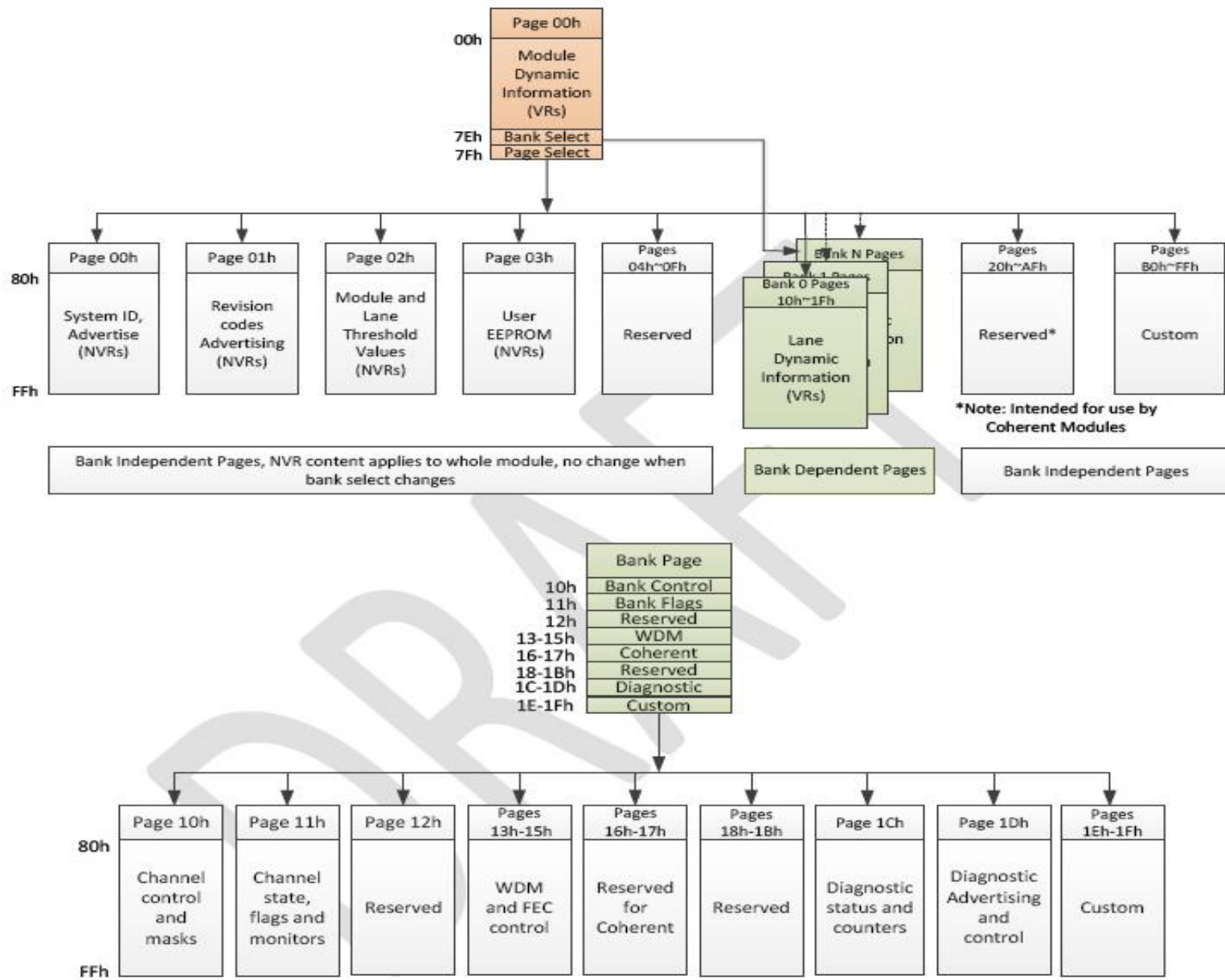


Figure 5. QSFP DD Memory Map

Mechanical Dimensions

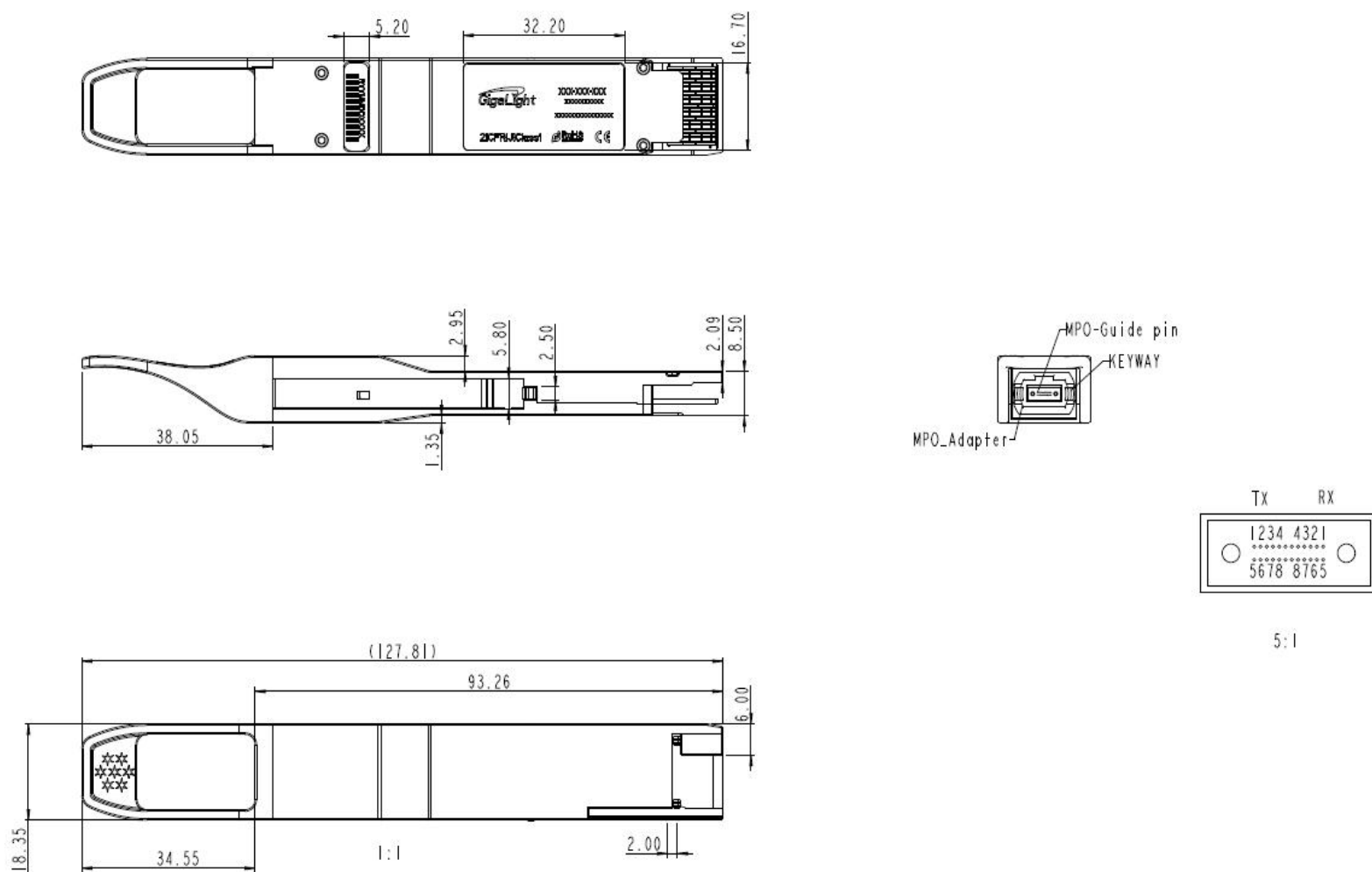


Figure 6. Mechanical Specifications



Regulatory Compliance

FiberStamp 400G transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (Third Edition)
Environmental protection	2011/65/EU
CE EMC	EN55032: 2015 EN55024: 2010+A1: 2015 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014
Product Safety	EN/UL 60950-1, 2nd Edition, 2014-10-14

References

1. QSFP DD MAS Rev4.0
2. CMIS V4.0
3. IEEE802.3cd 200GBASE-SR4
4. OIF CEI-56G-VSR-PAM4

⚠ CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FSTD-400G-SR8-A	400G QSFP-DD SR8, MPO24/PC
FSTD-400G-SR8-B	400G QSFP-DD SR8, MPO16/APC

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