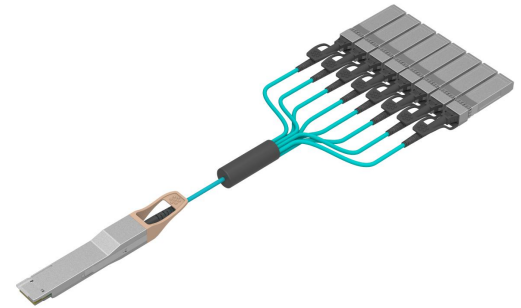# 400G QSFP56 DD to 8x53G SFP56 Breakout Active Optical Cable
## FYL8D-400MxxxC

## Features

- 8 channels full-duplex transceiver modules
- Transmission data rate up to 53Gbps per channel
- 8x53Gbps PAM4 transmitter and PM4 receiver
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Power consumption: <10W QSFP56 DD end;<2W SFP56 end
- Hot Pluggable QSFP DD form factor and Compliant with CMIS V4.0
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF with FEC
- Built-in digital diagnostic functions
- Operating case temperature 0℃ to +70℃
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

## Applications

- IEEE 802.3cd 200GBASE-SR4 and 50GBASE-SR

## Description

FIBERSTAMP 400G QSFP56 DD to 8x53G SFP56 breakout Active Optical Cable offers IT professionals a cost-effective interconnect solution for merging 400G QSFP56 DD and 53G SFP56 enabled host adapters, switches and servers.

For typical applications, users can install this splitter Active Optical cable between an available QSFP56 DD port on their 400Gbps rated switch and feed up to eight upstream 50GbE-SFP56 enabled switches. Each QSFP56 DD-SFP56 splitter Active Optical cable features a single QSFP56 DD connector (QSFP DD MSA) rated for 400Gbps on one end and (8) SFP56 connectors (SFF-8431), each rated for 53Gb/s, on the other.

This module incorporates FIBERSTAMP Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.
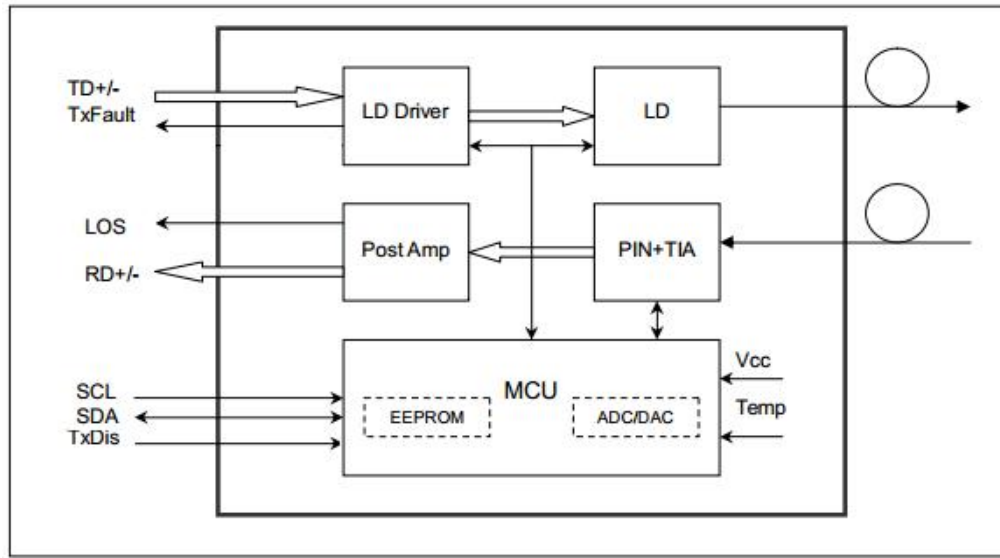
## QSFP56 DD end



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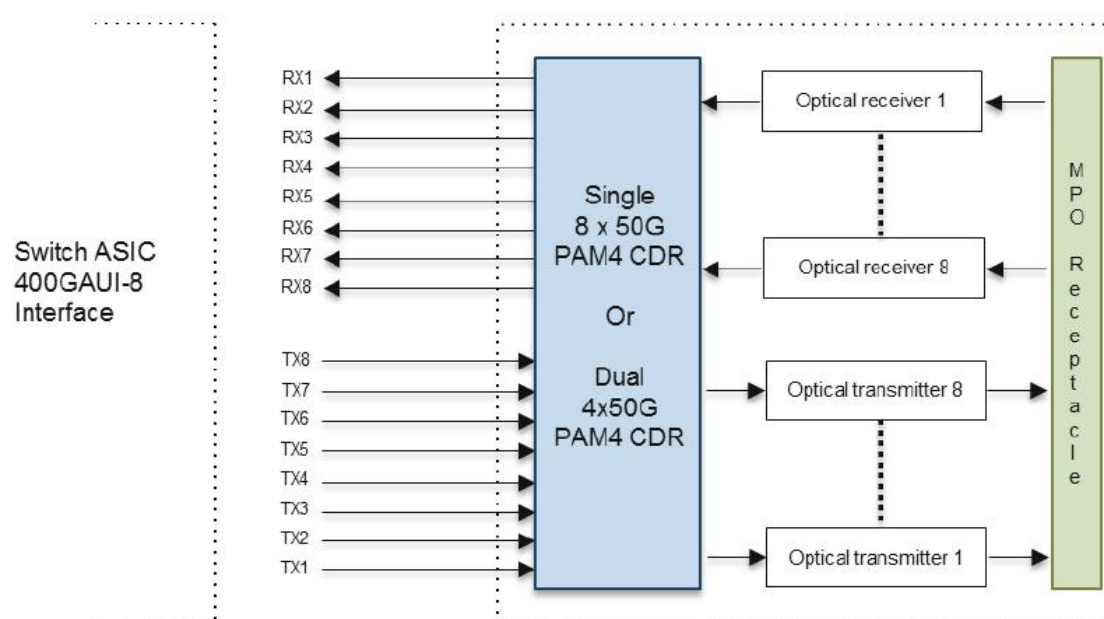
**SFP56 end**



**Figure1. Module Block Diagram**

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|-----------|--------|-----|-----|------|
| Supply Voltage | Vcc | -0.3 | 3.6 | V |
| Input Voltage | Vin | -0.3 | Vcc+0.3 | V |
| Storage Temperature | Tst | -20 | 85 | ℃ |
| Case Operating Temperature | Top | 0 | 70 | ℃ |
| Humidity(non-condensing) | Rh | 5 | 95 | % |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|-----------|--------|-----|---------|-----|------|
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Operating Case temperature | Tca | 0 | | 70 | ℃ |
| Data Rate Per Lane | fd | | 26.5325 | | GBd |
| Humidity | Rh | 5 | | 85 | % |
| Power Dissipation (QSFP56 DD end) | Pm | | | 10 | W |
| SFP56 per end | | | | 2 | W |

## Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|-----------|--------|-----|---------|-----|------|
| Differential input impedance | Zin | 90 | 100 | 110 | ohm |
| Differential Output impedance | Zout | 90 | 100 | 110 | ohm |
| Differential input voltage amplitude aAmplitude | ΔVin | | | 900 | mVp-p |
| Differential output voltage amplitude | ΔVout | | | 900 | mVp-p |
| Skew | Sw | | | 300 | ps |
| Bit Error Rate | BER | | | 2.4E-4 | - |
| Near-end Eye Width at $10^{-6}$ probability(EW6) | | 0.265 | | | UI |
| Near-end Eye Height at $10^{-6}$ probability(EH6) | | 70 | | | mV |
| Far-end Eye Width at $10^{-6}$ probability(EW6) | | 0.20 | | | UI |

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| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Far-end Eye Height at 10^-6 probability(EH6) | | 30 | | | mV |
| Near-end Eye Linearity | | 0.85 | | | - |

**Note：**

1. BER=2.4E-4; PRBS31Q@26.5625GBd. Pre-FEC

2. Differential input voltage amplitude is measured between TxnP and TxnN.

3. Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

### Table 3 - Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Centre Wavelength | λc | 840 | 850 | 860 | nm | - |
| RMS spectral width | Δλ | - | - | 0.6 | nm | - |
| Average launch power, each lane | Pout | -6 | - | 4 | dBm | - |
| Optical Modulation Amplitude (OMAouter), each lane | OMA | -4 | | 3 | dBm | - |
| Transmitter and dispersion eye closure(TDEC),each lane | TDEC | | | 4.9 | dB | |
| Extinction Ratio | ER | 3 | - | - | dB | - |
| Average launch power of OFF transmitter, each lane | | | | -30 | dB | - |
| **Receive** | | | | | | |
| Centre Wavelength | λc | 840 | 850 | 860 | nm | - |
| Receiver Sensitivity in OMAout | RXsen | | | -7 | dBm | 1 |
| Stressed Receiver Sensitivity in OMA out | | | | -3 | dBm | 1 |
| Maximum Average power at receiver , each lane input, each lane | | | | 4 | dBm | - |
| Minimum Average power at receiver , each lane | | -7.9 | | | dBm | |
| Receiver Reflectance | | | | -12 | dB | - |
| LOS Assert | | -10 | | | dBm | - |
| LOS De-Assert – OMA | | | | -7.5 | dBm | - |
| LOS Hysteresis | | 0.5 | | | dB | - |

**Note：**

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Per-FEC

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## Pin Description (QSFP56 DD end)

**Table 1- Pad Function Definition**

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1B | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B | |
| 4 | | GND | Ground | 1B | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B | |
| 7 | | GND | Ground | 1B | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3B | |
| 9 | LVTTL-I | ResetL | Module Reset | 3B | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3B | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3B | |
| 13 | | GND | Ground | 1B | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B | |
| 16 | | GND | Ground | 1B | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B | |
| 19 | | GND | Ground | 1B | 1 |
| 20 | | GND | Ground | 1B | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B | |
| 23 | | GND | Ground | 1B | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B | |
| 26 | | GND | Ground | 1B | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B | |
| 28 | LVTTL-O | IntL | Interrupt | 3B | |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2B | 2 |
| 31 | LVTTL-I | InitMode | Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE | 3B | |
| 32 | | GND | Ground | 1B | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B | |
| 35 | | GND | Ground | 1B | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B | |
| 38 | | GND | Ground | 1B | 1 |
| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
| 39 | | GND | Ground | 1A | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A | |
| 42 | | GND | Ground | 1A | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A | |
| 45 | | GND | Ground | 1A | 1 |
| 46 | | Reserved | For future use | 3A | 3 |
| 47 | | VS1 | Module Vendor Specific 1 | 3A | 3 |
| 48 | | VccRx1 | 3.3V Power Supply | 2A | 2 |
| 49 | | VS2 | Module Vendor Specific 2 | 3A | 3 |
| 50 | | VS3 | Module Vendor Specific 3 | 3A | 3 |
| 51 | | GND | Ground | 1A | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A | |
| 54 | | GND | Ground | 1A | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A | |
| 57 | | GND | Ground | 1A | 1 |
| 58 | | GND | Ground | 1A | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A | |
| 61 | | GND | Ground | 1A | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A | |
| 64 | | GND | Ground | 1A | 1 |
| 65 | | NC | No Connect | 3A | 3 |
| 66 | | Reserved | For future use | 3A | 3 |
| 67 | | VccTx1 | 3.3V Power Supply | 2A | 2 |
| 68 | | Vcc2 | 3.3V Power Supply | 2A | 2 |
| 69 | | Reserved | For Future Use | 3A | 3 |
| 70 | | GND | Ground | 1A | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A | |
| 73 | | GND | Ground | 1A | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A | |
| 76 | | GND | Ground | 1A | 1 |

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
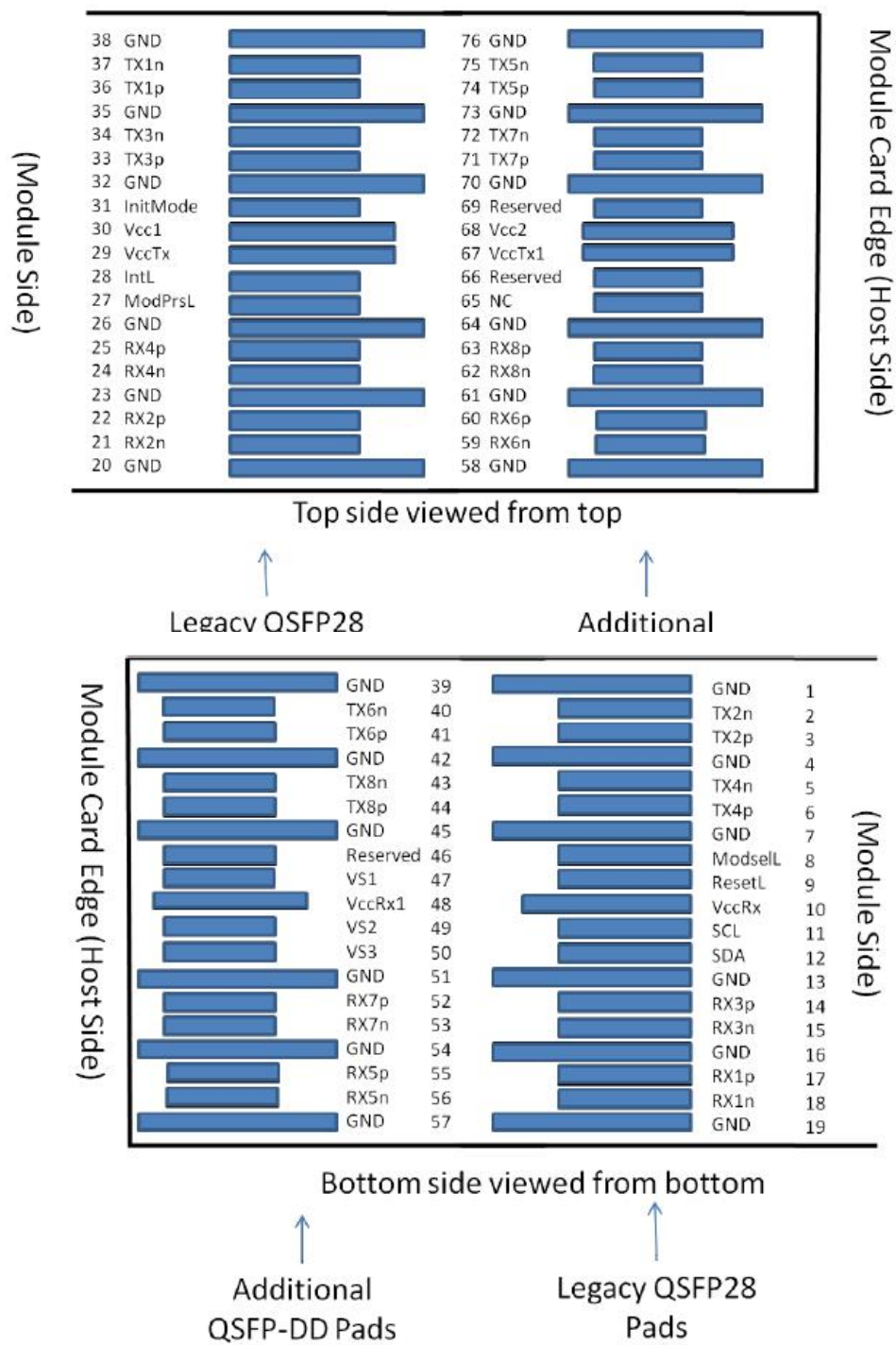
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**Figure2. Electrical Pin-out Details**

### ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

### ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See    Table 13 ) initiates a complete module reset, returning all user module settings to their default state.

### InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted

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Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

## ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

## IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

## Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.
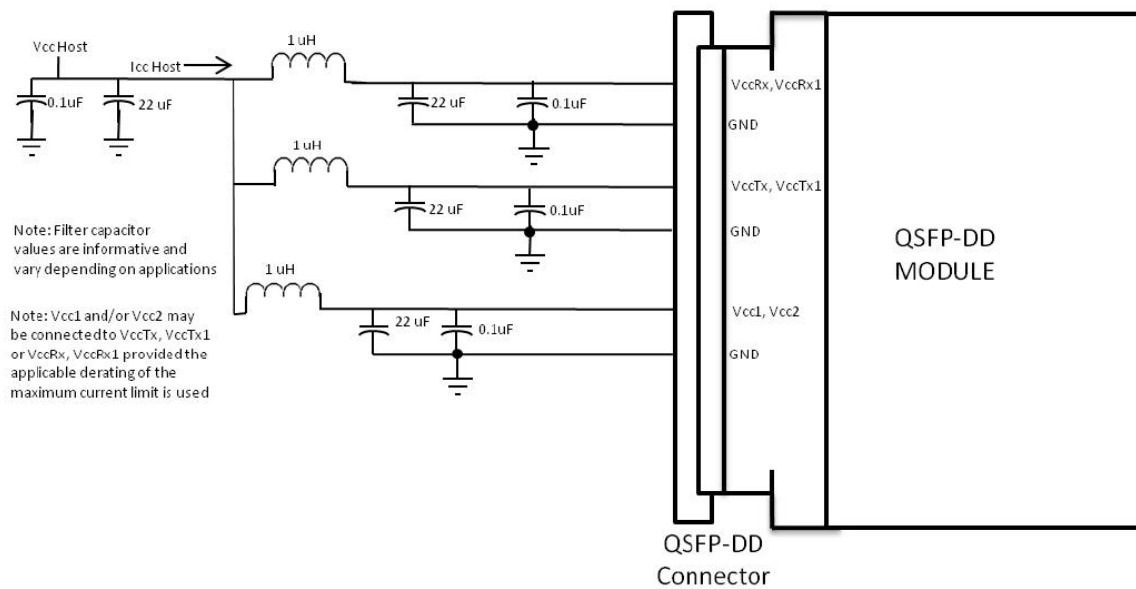


Figure3. Host Board Power Supply Filtering

## DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP DD products. A 2-wire serial interfaceprovides user to contact with module.

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital 3 monitoring and certain control functions. The interface is mandatory for all CMIS 4 devices. The interface has been designed largely after the QSFP memory map. The memory 5 map has been changed in order to accommodate 8 electrical lanes and limit the required 6 memory space. The single address approach is used as found in QSFP. Paging is used in 7 order to enable time critical interactions between host and module. 8

9 The structure of the memory is shown in Figure 4 . The memory space is arranged into a 10 lower, single page, address space of 128 bytes and multiple upper address space pages. 11 This structure supports a flat 256 byte memory for passive copper cables and permits 12 timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical 13 entries, e.g. serial ID information and threshold settings, are available with the Page 14 Select function. The structure also provides address expansion by adding additional upper 15 pages as needed. Upper pages 00-02 all contain static, non-volatile advertising 16 registers. Upper page 01 provides revision codes and advertising registers that indicate 17 the capabilities of the module. Upper page 02 provides thresholds for monitored 18 functions. Upper page 03 provides a user read/write space. The lower page and upper page 19 00 are required for passive copper cables and are always implemented. In addition, upper 20 pages 1, 2 and

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bank 0 pages 10h and 11h are required for active modules. See　CMIS Document Table 40　for 21 details regarding the implementation of optional upper pages and the bank pages. Bank 22 pages are provided to provide the ability to support modules with more than 8 lanes. Bank 23 0 provides lane-specific registers for the lower 8 lanes. Each additional bank provides 24 support for an additional 8 lanes. Reserved bytes are for future use and shall not be 25 used and shall be set to 0. Other organizations shall contact the managing organization 26 or the editor of this document to request allocations of registers. The use of custom 27 bytes is not restricted and may be vendor defined. The use of registers defined as custom 28 may be subject to additional agreements between module users and vendors.
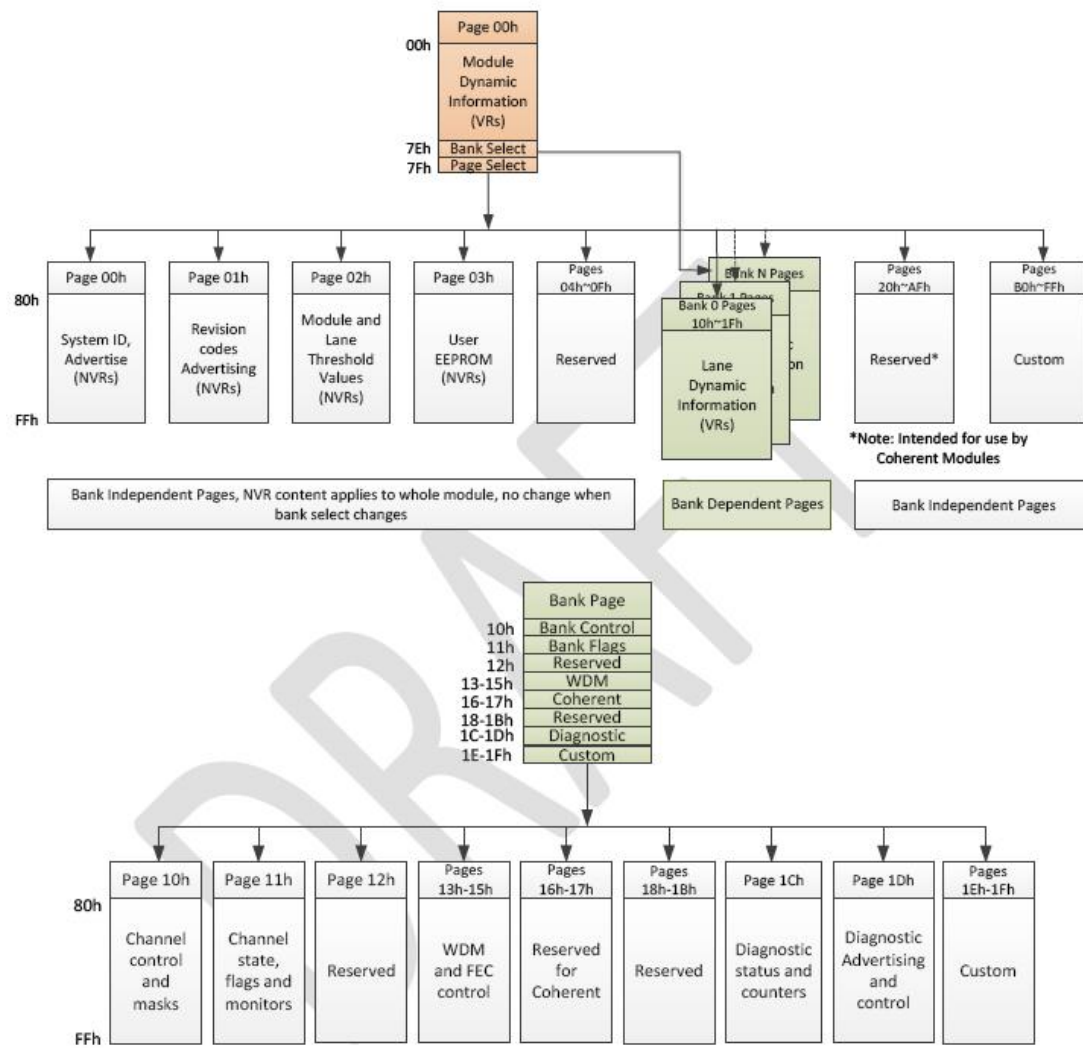


**Figure4. QSFP DD Memory Map**

## Pin Descriptions (SFP56 end)

| PIN | Logic | Symbol | Name / Description | Note |
|---|---|---|---|---|
| 1 | | VeeT | Module Transmitter Ground | 1 |
| 2 | LVTTL-O | TX_Fault | Module Transmitter Fault | 2 |
| 3 | LVTTL-I | TX_Dis | Transmitter Disable; Turns off transmitter laser output | |
| 4 | LVTTL-I/O | SDA | 2-Wire Serial Interface Data Line | 2 |
| 5 | LVTTL-I | SCL | 2-Wire Serial Interface Clock | 2 |
| 6 | | MOD_ABS | Module Definition, Grounded in the module | |
| 7 | LVTTL-I | RS0 | Receiver Rate Select | |
| 8 | LVTTL-O | RX_LOS | Receiver Loss of Signal Indication Active LOW | |
| 9 | LVTTL-I | RS1 | Transmitter Rate Select (not used) | |
| 10 | | VeeR | Module Receiver Ground | 1 |
| 11 | | VeeR | Module Receiver Ground | 1 |
| 12 | CML-O | RD- | Receiver Inverted Data Output | |
| 13 | CML-O | RD+ | Receiver Data Output | |
| 14 | | VeeR | Module Receiver Ground | 1 |
| 15 | | VccR | Module Receiver 3.3 V Supply | |
| 16 | | VccT | Module Receiver 3.3 V Supply | |

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| 17 | | VeeT | Module Transmitter Ground | 1 |
|----|-------|------|-------------------------------------|---|
| 18 | CML-I | TD+ | Transmitter Non-Inverted Data Input | |
| 19 | CML-I | TD- | Transmitter Inverted Data Input | |
| 20 | | VeeT | Module Transmitter Ground | 1 |

**Notes:**

1.  Module ground pins GND are isolated from the module case.

2.  Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

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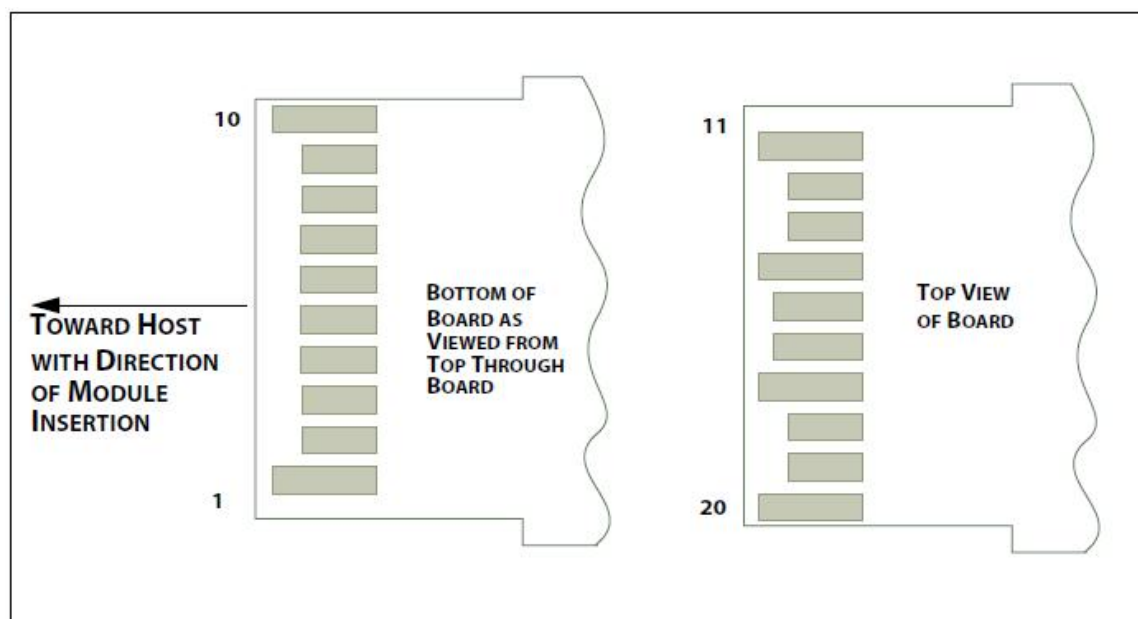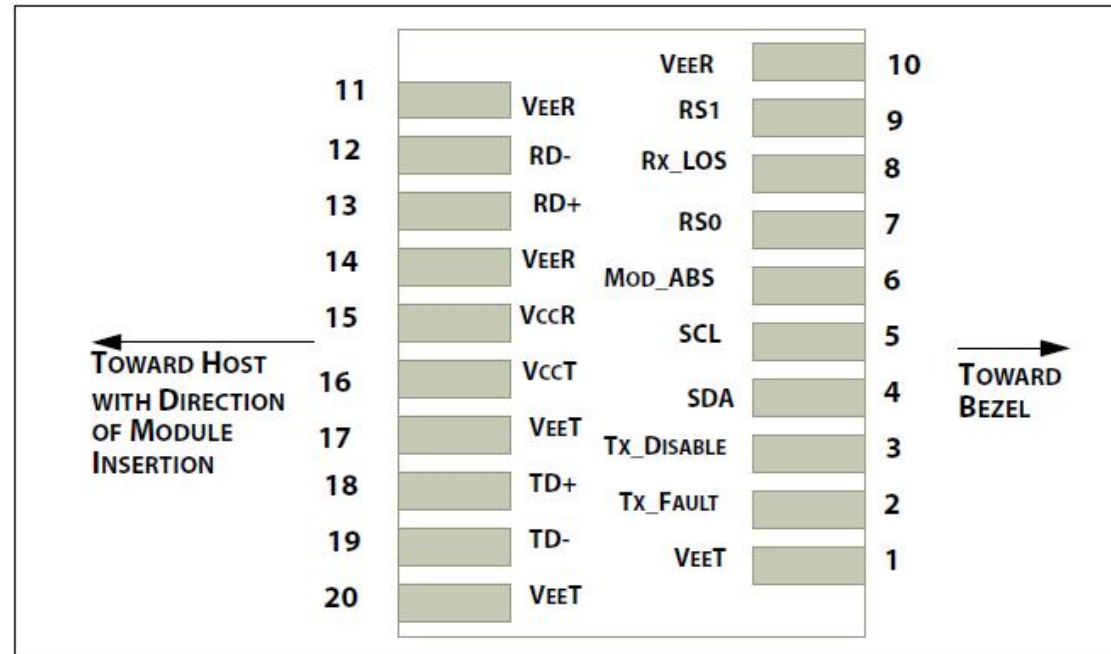
**Recommended Interface Circuit**
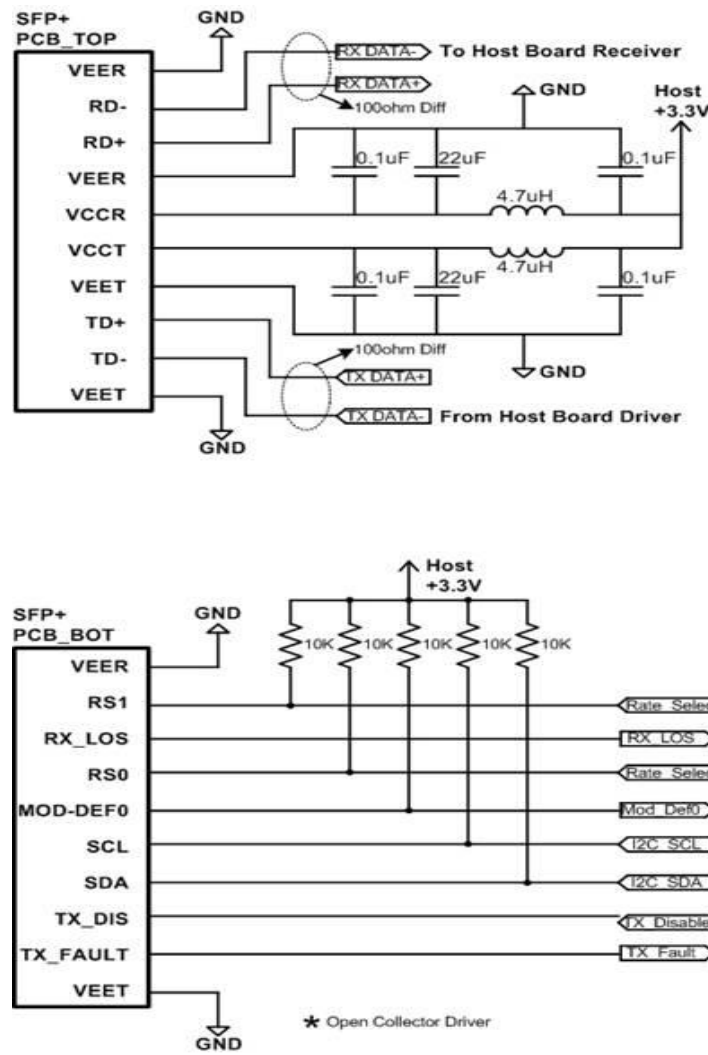




**Mechanical Dimensions**

**Digital Diagnostic Memory Map**

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following.

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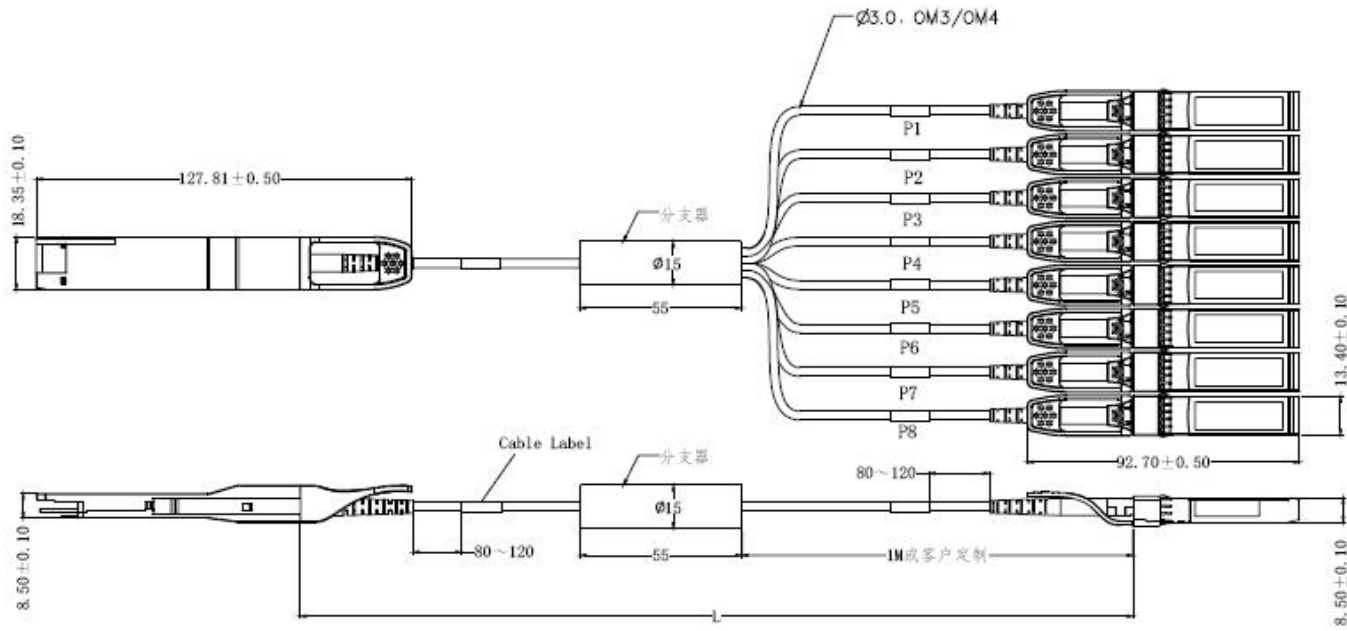FIBERSTAMP Co,.Ltd.
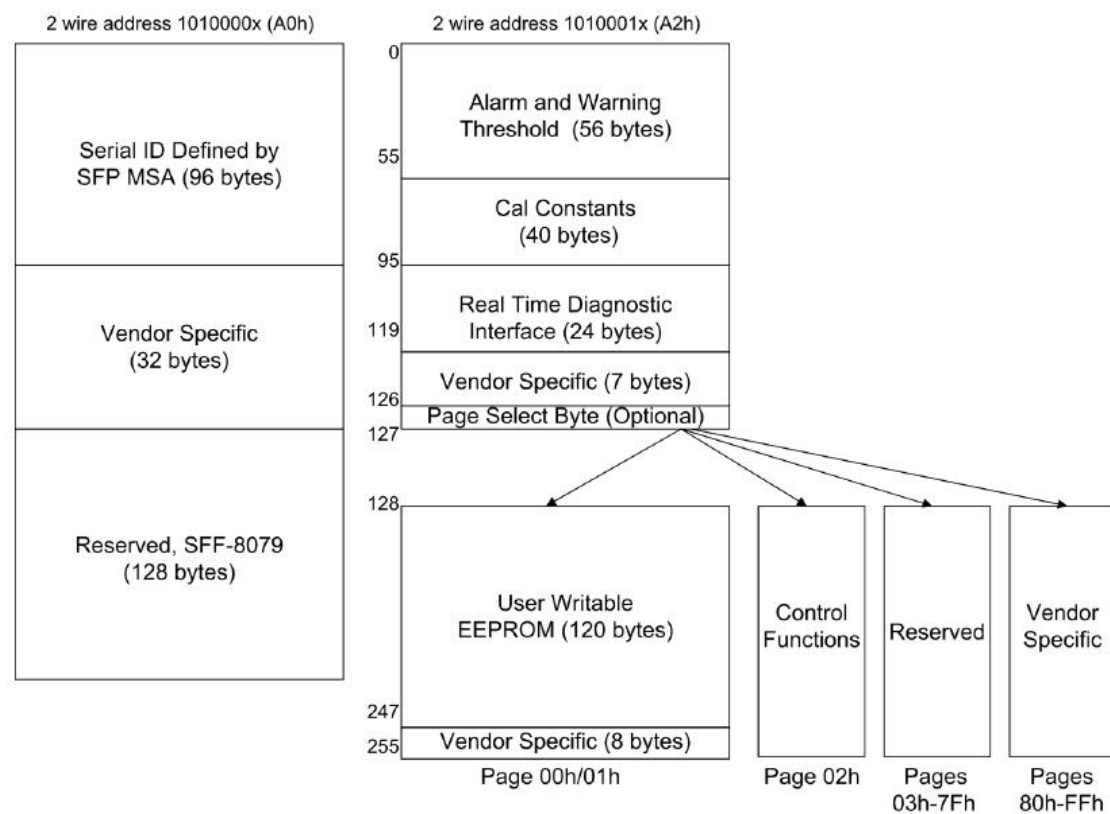
## Mechanical Dimensions



**Figure5. Mechanical Specifications**

## Regulatory Compliance

FIBERSTAMP FYL8D-400MxxxC 400G QSFP56 DD to 8*SFP56 AOC are Class 1 Laser Products. They are certified per the following standards:

| Feature | Standard |
|---|---|
| Laser Safety | IEC 60825-1:2014 (Third Edition) |
| Environmental protection | 2011/65/EU |
| CE EMC | EN55032：2015<br>EN55035：2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013 |
| FCC | FCC Part 15, Subpart B; ANSI C63.4-2014 |

## References

1. QSFP DD MAS Rev4.0

2. CMIS V4.0

3. IEEE802.3cd 200GBASE-SR4 50GBASE-SR

4. OIF CEI-56G-VSR-PAM4

5. SFP-8472 V12.3

6. SFP-8431

⚠️**CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Ordering information

| Part Number | Product Description |
|---|---|
| FYL8D-400MxxxC | 400G QSFP56 DD to 8x53G SFP56 AOC, 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF |
| xxx | 005-5m,  020-20m,  050-50m,  100-100m, |

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