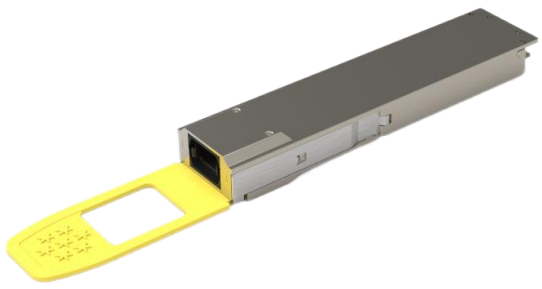
# FIBERSTAMP 400G OSFP-RHS DR4 500m Silicon Photonics Transceiver Module

## FUR-400P4M50C

**Features**

- OSFP MSA and CMIS compliant
- Compliant to 802.3bs
- 4x106.25Gbps(53.125GBd PAM4)electrical interface
- 4x106.25Gbps(53.125GBd PAM4)optics architecture
- Power consumption <10W
- Maximum link length of 500m G.652 SMF with KP-FEC
- MPO-12 receptacles
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS compliant(lead free)



**Applications**

- Ethernet and Telecom
- Infiniband

**Description**

The FIBERSTAMP FUR-400P4M50C is a transceiver module designed for 500m optical communication applications, and it is compliant to OSFP MSA, IEEE 802.3bs protocol. The silicon photonics transceiver is based on a new state-of-the-art silicon photonics (SiPh) platform. It uses SiPh chips that integrate a number of active and passive optoelectronic components, 3D packaging technology and industry-leading 7nm DSP chips. It is a cost-effective and lower power consumption solution for 400GBASE data center. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

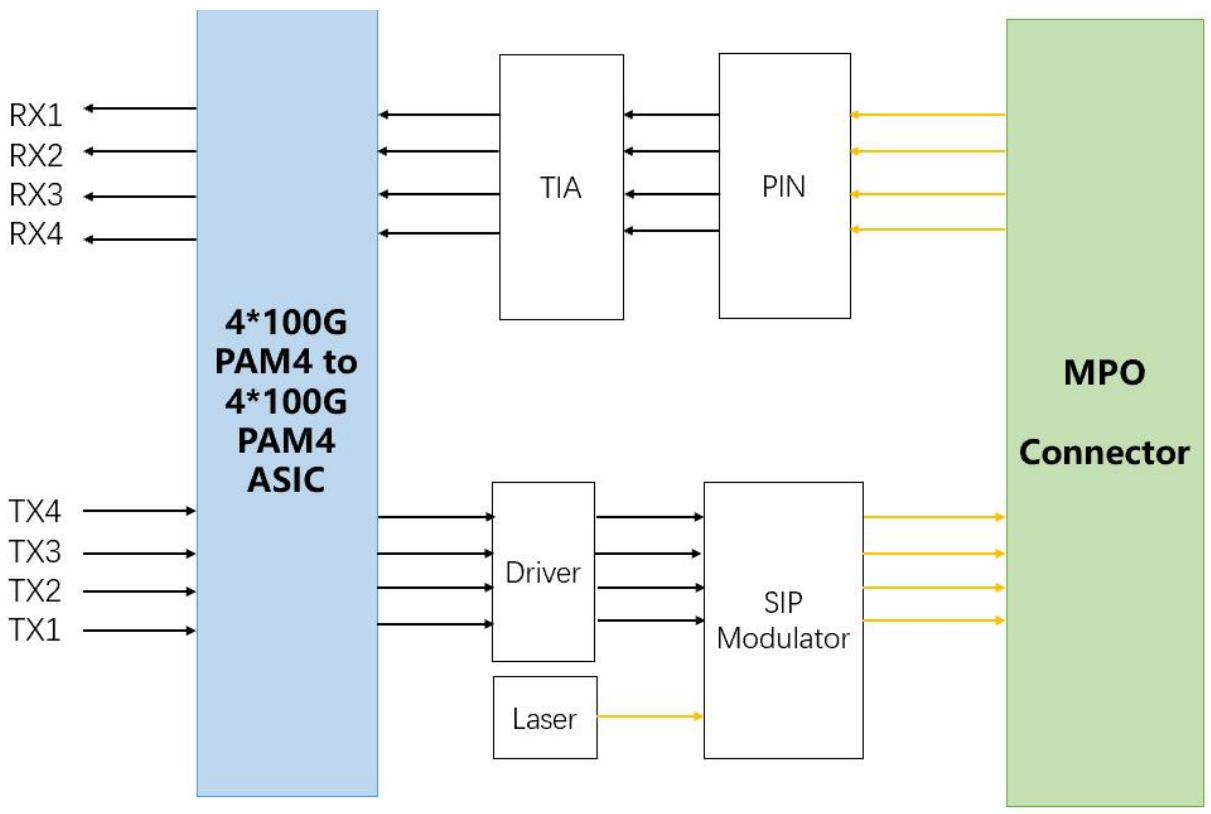



**Figure1. Module Block Diagram**

### Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | Vcc | -0.3 | 3.6 | V |
| Input Voltage | Vin | -0.3 | Vcc+0.3 | V |
| Storage Temperature | Tst | -40 | 85 | °C |
| Case Operating Temperature | Top | 0 | 70 | °C |
| Humidity(non-condensing) | Rh | 5 | 95 | % |

### Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Operating Case temperature | Tca | 0 | | 70 | °C |
| Data Rate Per Lane | fd | | 106.25 | | Gbit/s |
| Humidity | Rh | 15 | | 85 | % |
| Power Dissipation | Pm | | | 10 | W |

### Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Differential input impedance | Zin | 90 | 100 | 110 | ohm |
| Differential Output impedance | Zout | 90 | 100 | 110 | ohm |
| Differential input voltage amplitude | ΔVin | 900 | | | mVp-p |
| Differential output voltage amplitude | ΔVout | | | 900 | mVp-p |
| Bit Error Rate | BER | | | 2.4E-4 | - |
| Transition Time | | 8 | | | ps |
| Near-end Vertical Eye Closure over +/- 50 mUI (VEC) | | 12 | | | UI |
| Near-end Vertical Eye Opening over +/- 50 mUI (VEO) | | 20 | | | mV |
| Far-end Vertical Eye Closure over +/- 50 mUI (VEC) | | 12 | | | UI |
| Far-end Vertical Eye Opening over +/- 50 mUI (VEO) | | 15 | | | mV |

**Note：**

1) BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC

2) Differential input voltage amplitude is measured between TxnP and TxnN.

3) Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

### Table 3 - Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Centre Wavelength | λc | 1304.5 | | 1317.5 | nm | - |

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Side-mode suppression ratio | SMSR | 30 | - | -- | dB | - |
| Average launch power, each lane | Pout | -2.9 | - | 4.0 | dBm | - |
| Optical Modulation Amplitude(OMA outer), each lane | OMA | -0.8 | - | 4.2 | dBm | - |
| Transmitter and dispersion eye closure for PAM4 (TDECQ),each lane | TDECQ | | | 3.4 | dB | |
| Extinction Ratio | ER | 3.5 | - | - | dB | - |
| Average launch power of OFF transmitter, each lane | | | | -15 | dB | - |
| **Receiver** | | | | | | |
| Centre Wavelength | λc | 1304.5 | | 1317.5 | nm | - |
| Receiver Sensitivity in OMA outer | RXsen | | | -4.4 | dBm | 1 |
| Average power at receiver , each lane input, each lane | Pin | -5.9 | | 4 | dBm | - |
| Receiver Reflectance | | | | -26 | dB | - |
| LOS Assert | | -13 | | | dBm | - |
| LOS De-Assert | | | | -10 | dBm | - |
| LOS Hysteresis | | 0.5 | | | dB | - |

**Note：**

1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

## Pin Description

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| 1 | GND | Ground | | | 1 | |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 4 | GND | Ground | | | 1 | |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 7 | GND | Ground | | | 1 | |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 10 | GND | Ground | | | 1 | |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 13 | GND | Ground | | | 1 | |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 15 | VCC | +3.3V Power | | Power from Host | 2 | |
| 16 | VCC | +3.3V Power | | Power from Host | 2 | |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 18 | GND | Ground | | | 1 | |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 21 | GND | Ground | | | 1 | |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 24 | GND | Ground | | | 1 | |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 27 | GND | Ground | | | 1 | |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 30 | GND | Ground | | | 1 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 31 | GND | Ground | | | 1 | |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 34 | GND | Ground | | | 1 | |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 37 | GND | Ground | | | 1 | |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 40 | GND | Ground | | | 1 | |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 43 | GND | Ground | | | 1 | |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 45 | VCC | +3.3V Power | | Power from Host | 2 | |
| 46 | VCC | +3.3V Power | | Power from Host | 2 | |
| 47 | SDA | 2-wire Serial interface data | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 48 | GND | Ground | | | 1 | |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 51 | GND | Ground | | | 1 | |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 54 | GND | Ground | | | 1 | |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 57 | GND | Ground | | | 1 | |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 60 | GND | Ground | | | 1 | |

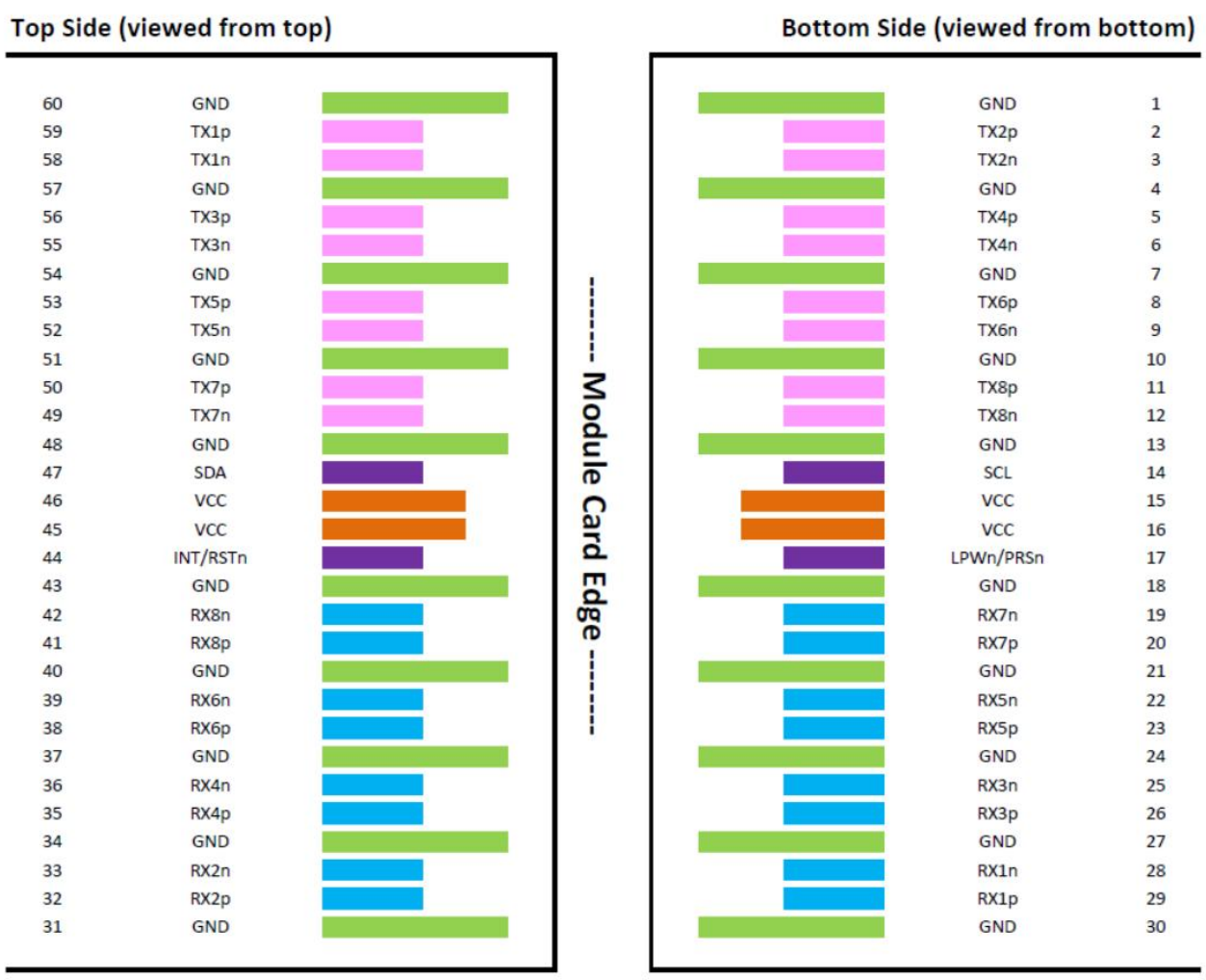



**Figure2. Electrical Pin-out Details**

**INT/RSTn Pin**

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 13-3 enables multilevel signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an activehigh signal on the module which gets translated to an active-high signal on the host. The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 13-2 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INT

signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

**LPWn/PRSn**

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 13-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an activelow signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 13-4 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

**Power Supply Filtering**

The host board should use the power supply filtering shown in Figure3.

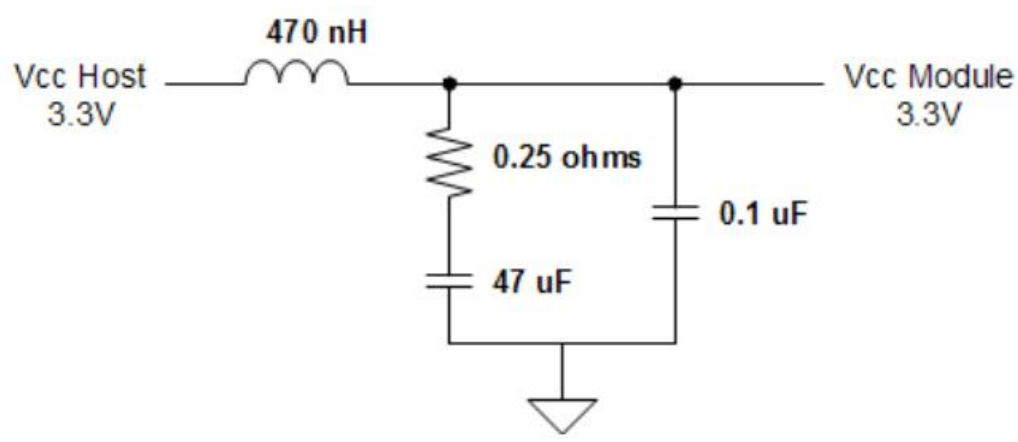



**Figure3. Host Board Power Supply Filtering**

**DIAGNOSTIC MONITORING INTERFACE**

Digital diagnostics monitoring function is available on all FIBERSTAMP OSFP products. A 2-wire serial interface provides user to contact with module.

**Memory Structure and Mapping**

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

**Note**: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 4 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

**Supported Pages**

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details

regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 4 lanes, and each additional bank provides support for additional 4 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 4 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

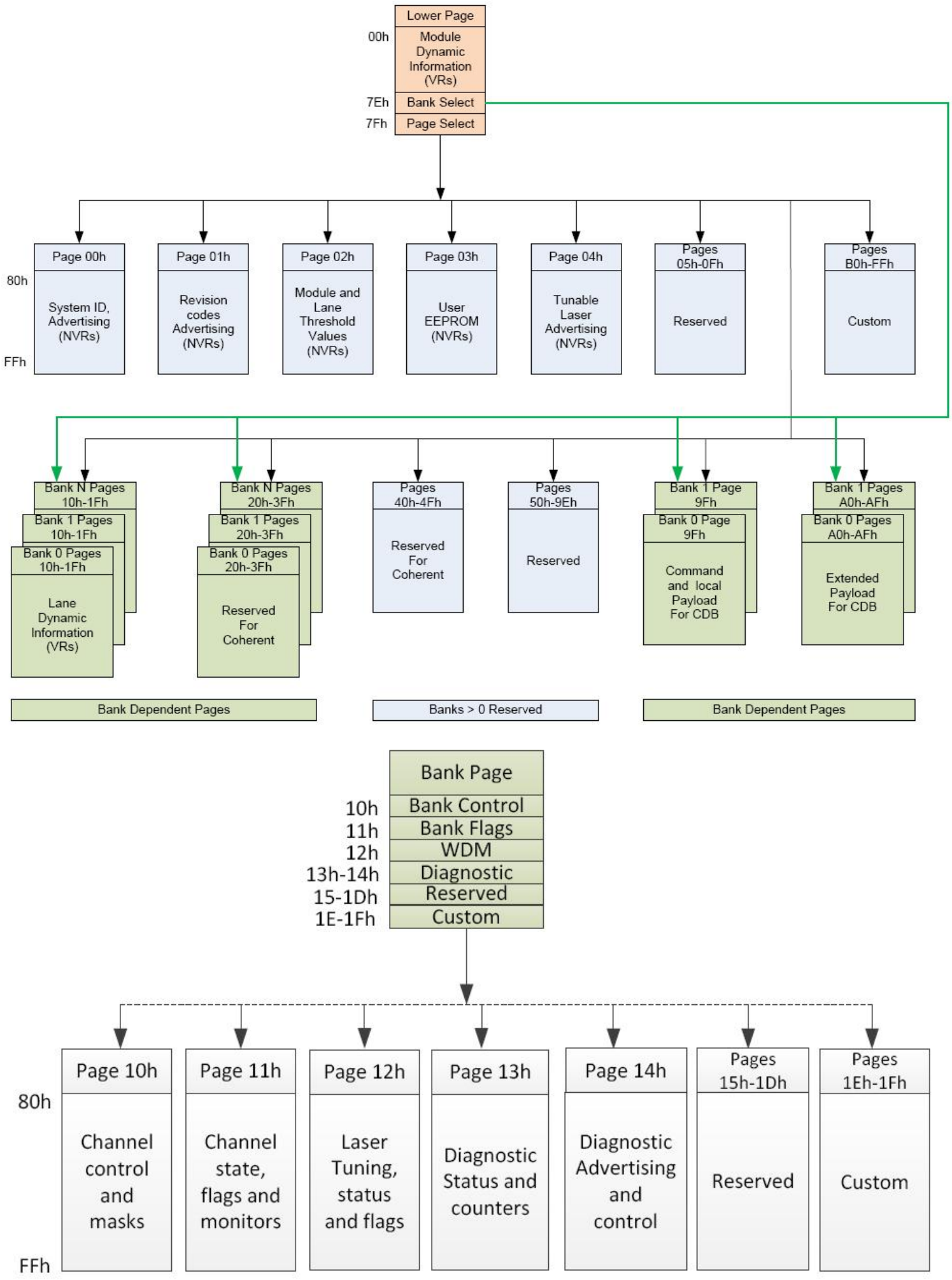



**Figure4. OSFP Memory Map**

## Mechanical Dimensions

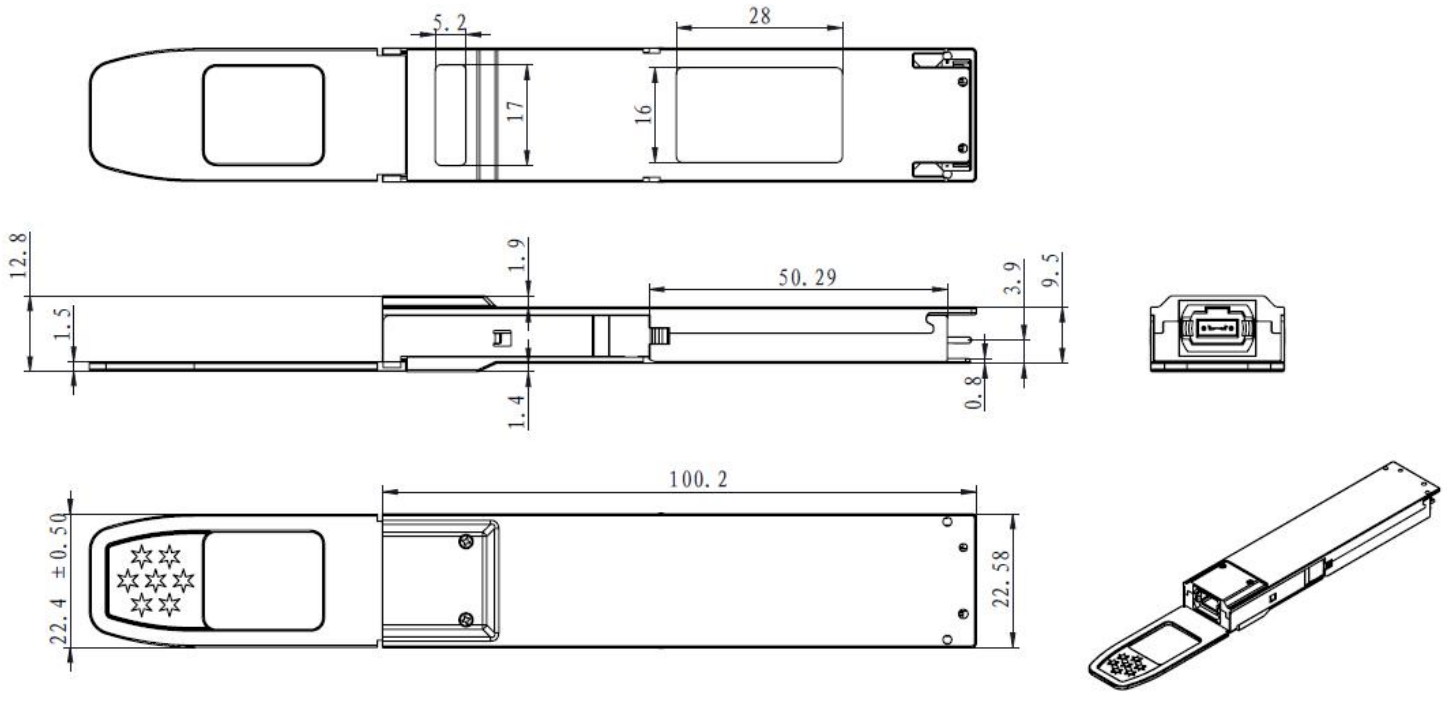



Figure5. Mechanical Specifications

## Regulatory Compliance

FIBERSTAMP FUR-400P4M50C transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

| Feature | Standard |
|---|---|
| Laser Safety | IEC 60825-1:2014 (3rd Edition)<br>IEC 60825-2:2004/AMD2:2010<br>EN 60825-1-2014<br>EN 60825-2:2004+A1+A2 |
| Electrical Safety | EN 62368-1: 2014<br>IEC 62368-1:2014<br>UL 62368-1:2014 |
| Environmental protection | Directive 2011/65/EU with amendment(EU)2015/863 |
| CE EMC | EN55032：2015<br>EN55035：2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013 |
| FCC | FCC Part 15, Subpart B<br>ANSI C63.4-2014 |

## References

1. OSFP MSA
2. CMIS
3. IEEE802.3bs
4. OIF CEI-112G-VSR

**⚠CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Ordering information

| Part Number | Product Description |
|---|---|
| FUR-400P4M50C | OSFP-RHS, 400GBASE-DR4, 500m on Single mode Fiber (SMF),with DSP Power consumption <10W, MPO-12 connector. |

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