400G CFP2 DCO Optical Transponder

FVN-400T75C60CY

Features

- Operating rate up to 425 Gbps
- PM-QPSK (200G) and PM-16QAM (200G / 400G) and PM-16QAM PS (200G) modulation formats
- 100GE, 200GE, 400GE and OTU4 / OTUCn services
- OTL4.4, FOIC1.4, CAUI-4 and FOIC1.2 electrical interfaces
- Near-end / remote-end data loopback
- CFP2 MSA Hardware Specification 1.0 with modifications compliant
- CFP MSA Management Interface Specification 2.2 with modifications compliant
- OTN framer and Ethernet MAC/PCS
- LLDP packet listening
- Hot-pluggable CFP2 form factor

General

The 400G CFP2-DCO coherent optical module uses a 104-pin CFP2-MSA electrical connector for connecting the host card. Figure1-1 shows the picture of this module.

Figure 1-1 Picture of the Module

The optical module consists of three functional parts: TX module, RX module and control module. All the control interface pins are provided by an internal micro controller. This micro controller can also be used for modulator control, software management, and alarm / performance event reporting. Figure 1-2 shows the block diagram of the 400G CFP2-DCO coherent optical module.

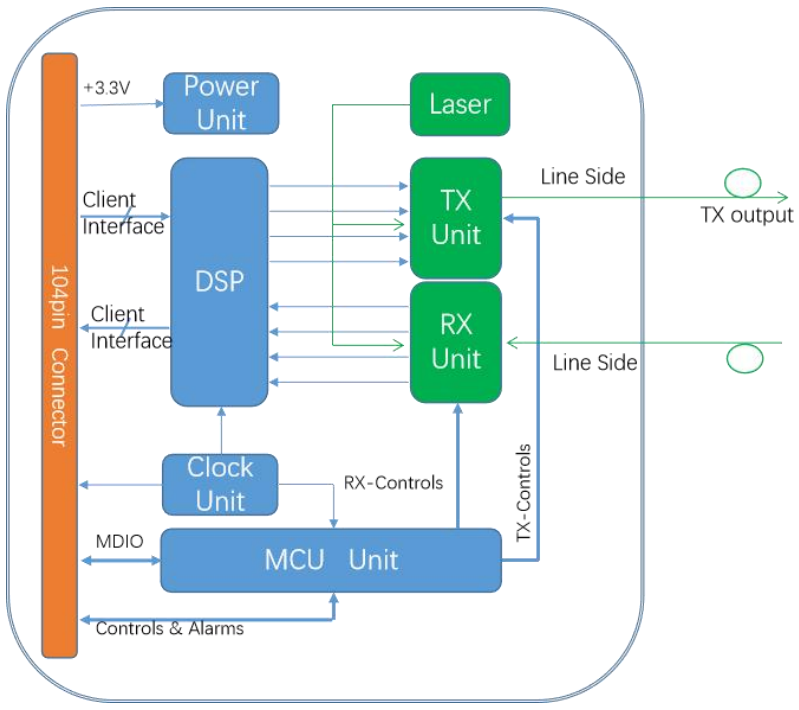

Figure 1-2 Module Block Diagram

Application

The 400G CFP2-DCO coherent optical module is used on the host system for MAN DWDM applications.

Performance Specifications
200G Optical Port

Table 4-1 200G PM-QPSK Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-QPSK
Optical channels	80
Grid spacing	75 GHz
Frequency range	190.7 to 196.65 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dB
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
Max. average DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	14.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 26 WMaximum: 28 W

Table 4-2 200G PM-16QAM Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-16QAM
Optical channels	96
Grid spacing	50 GHz
Frequency range	191.3 to 196.05 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-2.5 dBm
Max. Tx output power	-2.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
Max. average DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	18.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 WMaximum: 24 W

Table 4-3 200G PM-16QAM PS Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-16QAM PS
Optical channels	96
Grid spacing	50 GHz
Frequency range	191.3 to 196.05 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-2.5 dBm
Max. Tx output power	-2.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
Max. average DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	16.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 WMaximum: 24 W

400G Optical Port

Table 4-4 400G Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-16QAM
Optical channels	80
Grid spacing	75 GHz
Frequency range	190.7 to 196.65 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-2.5 dBm
Max. Tx output power	-2.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±15 000 ps/nm
Max. average DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	23 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 26 WMaximum: 28 W

Electrical Characteristics
Power Supply Requirements

The 400G CFP2-DCO coherent optical module is powered by an independent 3.3 V power supply on the host. All voltages are tested at the connector interfaces. Table 4-5 describes the power supply requirements.

Table 4-5 Coherent CFP2 Optical Module Power Supply Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
3.3 V DC power supply voltage	VCC	3.2	3.3	3.4	V	-
3.3 V DC power supply current	ICC	-	-	8.5	A	Note 1 & 2
Power supply noise	Vrip	-	-	2	%p-p	DC - 1 MHz
				3		1 - 10 MHz
Power consumption	Pw_class 4	-	26	28	W	400G mode
Operating temperature	T	0	-	70	°C	-

Note:

1. The Min. and Max. values apply to the full temperature range at the EOL of the module. Typical values (Typ.) are defined at the BOL of the module, with operating temperature at 25°C and expected power supplied.
2. The maximum current of each pin cannot exceed 1.3 A.
3. The Max. value of ICC is for design reference, and the expected working current cannot exceed Pw_normal/VCC.

High-Speed Electrical Interface Specifications

The 400G CFP2-DCO coherent optical module provides multiple electrical interfaces. For details, see Table 4-6.

Table 4-6 Coherent CFP2 Optical Module

Client Type	Interface Type	Electrical Standards
100GE	CAUI-4	IEEE 802.3bm CAUI-4, Chip-to-Module
100GE	100GAUI-2	IEEE 802.3bm GAUI-8 Chip-to-Module
200GE	200GAUI-8	OIF CEI-28G VSR
200GE	200GAUI-4	IEEE 802.3bm GAUI-8, Chip-to-Module
400GE	400GAUI-8	-
OTU4	OTL4.4	OIF CEI-28G VSR
OTU4	OTL4.2	OIF CEI-56G VSR PAM-4
OTUC1 / OTUC2	FOIC1.4 (FlexO-SR)	OIF CEI-28G VSR
OTUC1 / OTUC2 / OTUC3 / OTUC4	FOIC1.2 (FlexO-SR)	OIF CEI-56G VSR PAM-4

Reference Clock (REFCLK)

The host does not need to provide a reference clock (REFCLK) for the 400G CFP2-DCO coherent optical module.

Transmitter Monitor Clock (TXMCLK)

The transmitter of the 400G CFP2-DCO coherent optical module provides a monitoring clock TXMCLK, which is mainly used as a reference for monitoring optical signals at the transmitter. This clock can be used to trigger a high-speed sampling oscilloscope.

Table 4-7 Performance Specifications of the Transmitter Monitor Clock (TXMCLK)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Impedance	Zd	80	100	120	Ω	-
Transmitter monitor clock frequency (TXMCLK)	-	-	1/48	-	Hz	The frequency is 1/48 the symbol rate of the transmitter's optical signal.
TXMCLK differential voltage	VDIFFTX	500	-	1000	mVppd	Differential peak-to-peak voltage

Control Pins (non-MDIO) Functional Description

TX_DIS (Transmitter Disable)

TX_DIS is an input pin which receives signals from the host and operates in the logic high state. When TX_DIS is logic high, the output optical signal inside the optical module is turned off. When TX_DIS is logic low, the output optical signal inside the optical module is turned on. Figure 4-1 shows the timing diagram for "t_on" (turn-on time) and "t_off" (turn-off time).

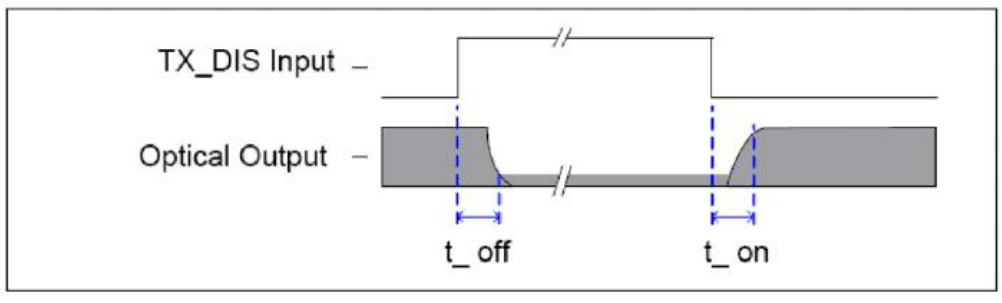

Figure 4-1 Timing Diagram for TX_DIS

MOD_LOPWR (Module Low Power)

MOD_LOPWR is an input pin which receives signals from the host and works in the logic high state. When MOD_LOPWR is logic high, the optical module works at low power consumption and remains in this mode. When MOD_LOPWR is pulled down, the optical module is initialized to a high power consumption state, that is, the normal operation mode. In low power consumption mode, the optical module communicates through the MDIO management interface, and its maximum power consumption does not exceed 2 W. Figure 4-2 shows the timing diagram for "t_MOD_LOPWR_on" and "t_MOD_LOPWR_off".

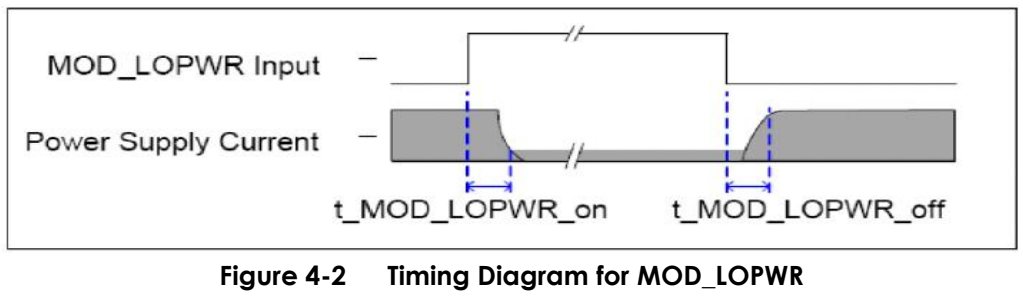

Figure 4-2 Timing Diagram for MOD_LOPWR

MOD_RSTn (Module Reset)

MOD_RSTn is an input pin which receives signals from the host and works in the logic low state. When MOD_RSTn is pulled low, the optical module is in the reset state. When MOD_RSTn is logic high, the optical module exits the reset mode and starts power-on initialization.

Alarm Pins (non-MDIO) Functional Description

RX_LOS (Receiver Loss of Signal)

RX_LOS is an output pin which transmits signals to the host and works at the logic high state. When RX_LOS is logic high, the optical power received by the optical module is too low. Figure 4-3 shows the timing diagram for RX_LOS.

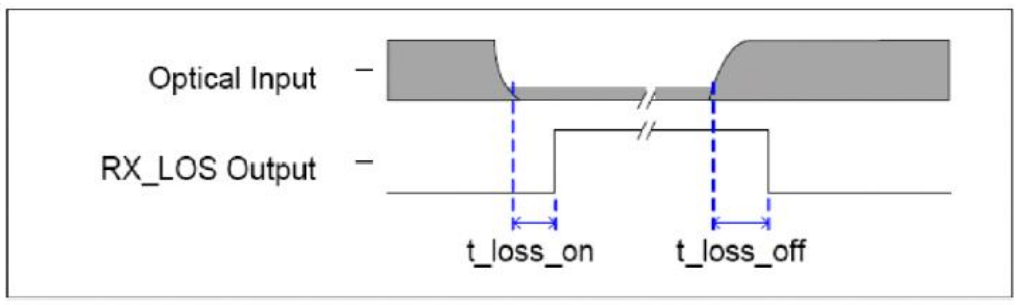

Figure 4-3 Timing Diagram for RX_LOS

MOD_ABS (Module Absent)

MOD_ABS is an output pin which transmits signals from the inside of the module to the host. This pin is pulled up on the host and pulled down to the ground inside the module. When the optical module is inserted into the host, MOD_ABS is logic low, meaning that the module is present. When the optical module is absent on the host, MOD_ABS is logic high, meaning that the module is absent.

Control and Alarm Descriptions

Timing Parameters for Control and Alarm Signals

Table 4-8 Timing Parameters for Control and Alarm Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter Disabled (TX_DIS high)	t_off	-	-	1	ms
Transmitter Enabled (TX_DIS low)	t_on	-	-	25	s
MOD_LOPWR assert	t_MOD_LOPWR_assert	-	-	25	s
MOD_LOPWR deassert	t_MOD_LOPWR_deassert	-	-	25	s
Receiver Loss of Signal Assert Time	t_loss_on	-	-	1	ms
Receiver Loss of Signal De-assert Time	t_loss_off	-	-	15	ms
Initialization time from Reset	t_initialize	190	-	220	s

3.3 V LVCMOS Electrical Characteristics

The 3.3 V LVCMOS level of the hardware control and alarm signal pins described above shall meet the electrical characteristics described in Table 4-9. Figure 4-4 shows the recommended input and output termination modes for these pins.

Table 4-9 3.3 V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	3.2	3.3	3.4	V
Input high voltage	VIH	2	-	VCC+0.3	V
Input low voltage	VIL	-0.3	-	0.8	V
Input leakage current	IIN	-10	-	10	µA
Output high voltage (IOH = -100 µA)	VOH	VCC-0.2	-	-	V
Output low voltage (IOL = 100 µA)	VOL	-	-	0.2	V

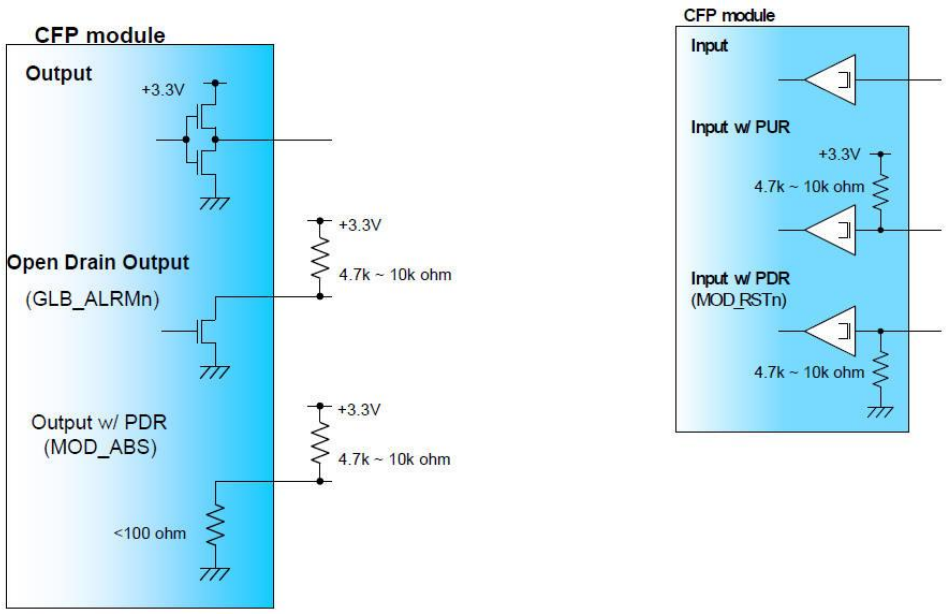

Figure 4-4 Reference 3.3 V LVCMOS Input / Output Termination

Module Management Interface Pins (MDIO) Description
Management Data Input / Output (MDIO) Interface

The MDIO implementation is defined in IEEE 802.3 clause 45. The MDIO of the optical module uses the 1.2 V LVCMOS logic level.

Management Data Clock (MDC) Interface Pins

Figure 4-5 shows the timing diagram for the MDIO and MDC pins. The optical module should follow the minimum setup time "tsetup" and hold time "thold" requirements of the MDIO port supplementary protocol.

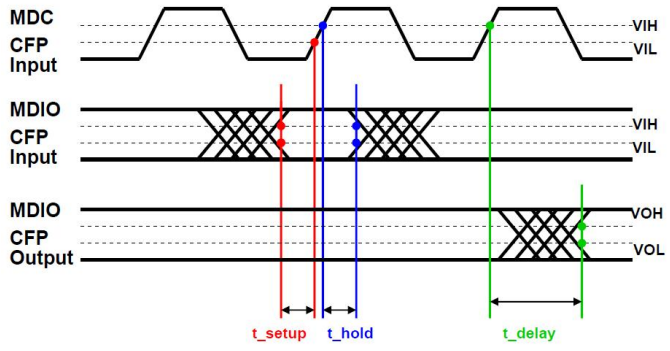

Figure 4-5 Timing Diagram for the MDIO & MDC Interfaces

Note: Tested on the MDIO & MDC pins of the optical module.

MDIO Physical Port Address Pins (PRTADRs)

The PRTADRs are used by the host system to assign addresses to all optical modules belonging to its management area. PREADR0 corresponds to the LSB of the physical port address bit. The host drives the physical port address line of 5pin to set the physical port address of the optical module by following the address protocol of the MDIO port. It is recommended that these physical port addresses should not change when the optical module is powered on.

1.2 V LVCMOS Electrical Characteristics

Table 4-10 describes the electrical characteristics of the aforesaid MDIO pins operating in 1.2 V LVCMOS mode. Figure 4-6 shows the recommended input and output termination modes of these pins.

Table 4-10 1.2 V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input high voltage	VIH	0.84	-	1.5	V
Input low voltage	VIL	-0.3	-	0.36	V
Input leakage current	IIN	-100	-	100	μA
Output high voltage (IOH = -100 μA)	VOH	1	-	1.5	V
Output low voltage (IOL = 100 μA)	VOL	-0.3	-	0.2	V
Output high current	IOH	-	-	-4	mA
Output low current	IOL	+4	-	-	mA
Input capacitance	Ci	-	-	10	pF

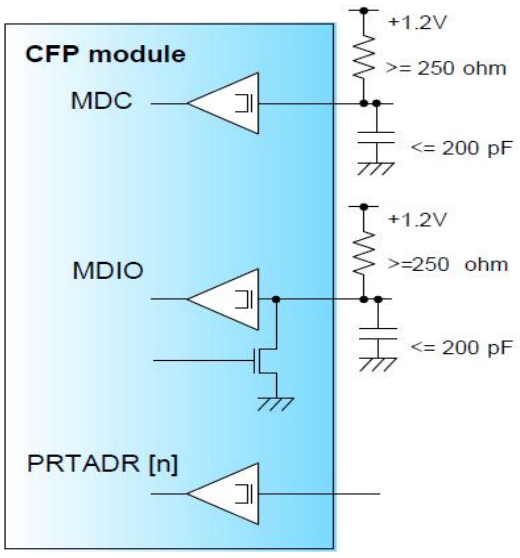

Figure 4-6 Reference MDIO Interface Termination

Mechanical Specifications

Figure 5-1 shows the mechanical dimensions of the 400G CFP2-DCO coherent optical module.

Max. dimensions (L × W × H): 109.5 mm × 42.5 mm × 15.4 mm

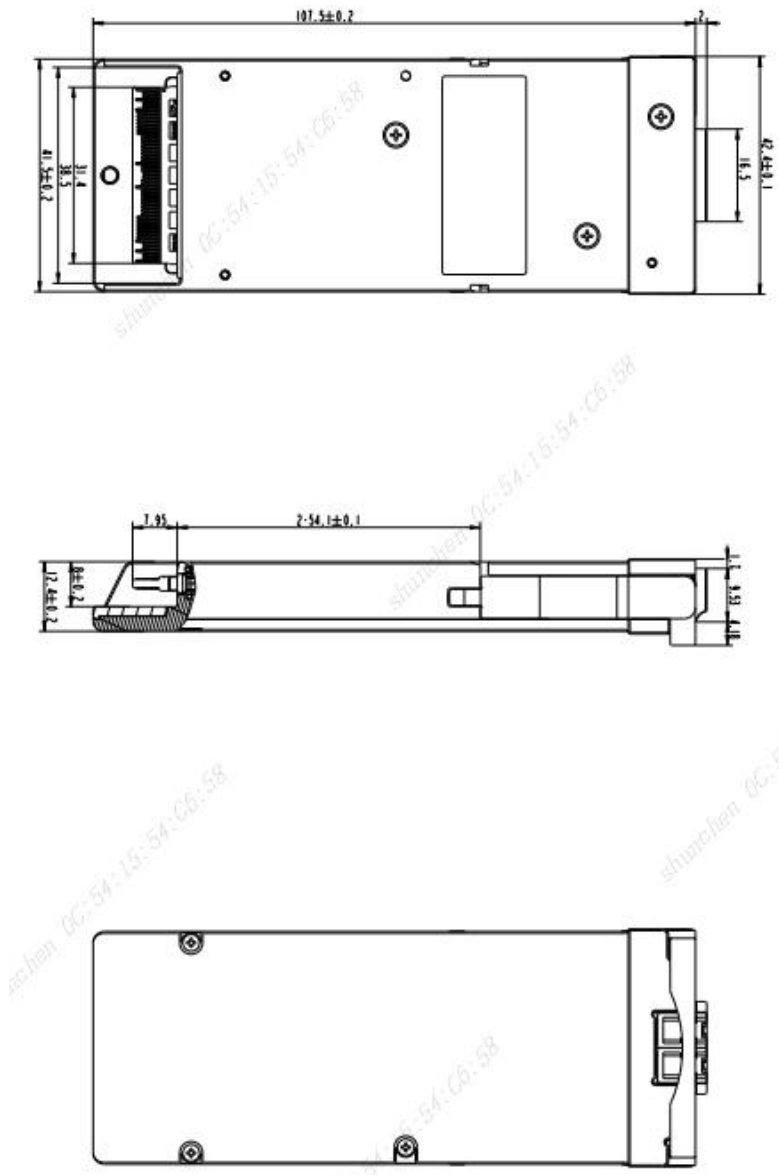

Figure 5-1 Mechanical Dimensions of the CFP2 Optical Module

Operating Environment

Table 6-1 Operating Environment

Parameter	Min.	Max.	Unit
Storage temperature	-40	85	℃
Operating case temperature	0	70	℃
Relative humidity, operating (non-condensing)	5	85	%
Relative humidity, operating (short term < 96 hrs, non-condensing)	5	95	%
ESD sensitivity (HBM)	-	High-speed pins: 500Other pins: 2000	V

Pin Assignment and Description

The electrical connection of 104pin includes eight pairs of TX differential signals (these signals are the input TXIs of the module, which connect to the signal outputs of the card), eight pairs of RX differential signals (these signals are the output RXOs of the module, which connect to the signal inputs of the card), a pair of monitoring clocks in the Tx direction, control pins, alarm pins, MDIO communication related pins, GND and +3.3 V power supply. The +3.3 V power supply supports a maximum overcurrent capacity of 1.3 A per pin.

Table 7-1 Pin Assignment (Non-High Speed Pins)

Pin	Bottom	I/O	Logic	Comment
1	GND	GND	Ground	Module Ground. Logic and power return path
2	OHIO_RDn	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
3	OHIO_RDp	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
4	GND	GND		Module Ground. Logic and power return path
5	OHIO_TD0n	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
6	OHIO_TD0p	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
7	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
8	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
9	3.3V	PWR		
10	3.3V	PWR		
11	3.3V	PWR		
12	3.3V	PWR		
13	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
14	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
15	VND_IO_A	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
16	VND_IO_B	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
17	PRG_CNTL1	I	LVCMOS w/PUR	Internal 10k pull-up; TRXIC_RSTn
18	PRG_CNTL2	I	LVCMOS w/PUR	Internal 10k pull-up; Hardware Interlock LSB
19	PRG_CNTL3	I	LVCMOS w/PUR	Internal 10k pull-up; Hardware Interlock MSB
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default “H” = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default “H” = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 2; MSA Default “H” = MOD_READY
23	GND	GND	Ground	Module Ground. Logic and power return path
24	TX_DIS	I	LVCMOS w/PUR	Transmitter disabled for all lanes. Internal 10k pull-up;
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal; Internal 4.7k pull-up.
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power; Internal 10k pull-up;
27	MOD_ABS	O	GND	Module Absent; Internal 50Ω pull-down;
28	MOD_RSTn	I	LVCMOS w/PDR	Module Reset; Internal 10k pull-down;
29	GLB_ALRMn	O	LVCMOS	Global Alarm “H” = Alarm; “L” = OK
30	GND	GND	Ground	Module Ground. Logic and power return path
31	MDC	I	1.2V CMOS	MDIO Clock input
32	MDIO	I/O	1.2V CMOS	Management Data Input Output.
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
37	VND_IO_D	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
38	VND_IO_E	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
39	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
40	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
41	3.3V	PWR		
42	3.3V	PWR		
43	3.3V	PWR		
44	3.3V	PWR		
45	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
46	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
47	NC	NC	NC	
48	NC	NC	NC	
49	GND	GND	Ground	Module Ground. Logic and power return path
50	TXMONCLKN	O	CML	For optical waveform testing. Not for normal use
51	TXMONCLKP	O	CML	For optical waveform testing. Not for normal use
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 7-2 Pin Assignment (High-speed Pins)

Pin	Top	I/O	Logic	Comment
104	GND	GND	Ground	Module Ground. Logic and power return path
103	TX4n	I	CML	
102	TX4p	I	CML	
101	GND	GND	Ground	Module Ground. Logic and power return path
100	TX3n	I	CML	
99	TX3p	I	CML	
98	GND	GND	Ground	Module Ground. Logic and power return path
97	TX2n	I	CML	
96	TX2p	I	CML	
95	GND	GND	Ground	Module Ground. Logic and power return path
94	TX5n	I	CML	
93	TX5p	I	CML	
92	GND	GND	Ground	Module Ground. Logic and power return path
91	TX6n	I	CML	
90	TX6p	I	CML	
89	GND	GND	Ground	Module Ground. Logic and power return path
88	TX1n	I	CML	
87	TX1p	I	CML	
86	GND	GND	Ground	Module Ground. Logic and power return path
85	TX0n	I	CML	
84	TX0p	I	CML	
83	GND	GND	Ground	Module Ground. Logic and power return path
82	TX7n	I	CML	
81	TX7p	I	CML	
80	GND	GND	Ground	Module Ground. Logic and power return path
79	(REFCLKn)	I	CML	
78	(REFCLKp)	I	CML	
77	GND	GND	Ground	Module Ground. Logic and power return path
76	RX4n	O	CML	
75	RX4p	O	CML	
74	GND	GND	Ground	Module Ground. Logic and power return path
73	RX3n	O	CML	
72	RX3p	O	CML	
71	GND	GND	Ground	Module Ground. Logic and power return path
70	RX2n	O	CML	
69	RX2p	O	CML	
68	GND	GND	Ground	Module Ground. Logic and power return path
67	RX5n	O	CML	
66	RX5p	O	CML	
65	GND	GND	Ground	Module Ground. Logic and power return path
64	RX6n	O	CML	
63	RX6p	O	CML	
62	GND	GND	Ground	Module Ground. Logic and power return path
61	RX1n	O	CML	
60	RX1p	O	CML	
59	GND	GND	Ground	Module Ground. Logic and power return path
58	RX0n	O	CML	
57	RX0p	O	CML	
56	GND	GND	Ground	Module Ground. Logic and power return path
55	RX7n	O	CML	
54	RX7p	O	CML	
53	GND	GND	Ground	Module Ground. Logic and power return path

Ordering Information

Model	Description
FVN-400T75C60CY	400G coherent CFP2-DCO

Revision History

Revision	Date	Changes
V0	Aug. 18th, 2022	New release.