25Gbps LAN-WDM SFP28 I-Temp Transceiver

FBC-D25LxxK40T

Features

- Hot-pluggable SFP28 Form Factor
- Supports 25.78Gb/s bit rate
- Supports 24.33Gb/s bit rate
- Transmitter: Cooled EML TOSA
- Receiver: APD ROSA
- Internal CDR circuits on receiver and transmitter

- < 1.8W power dissipation
- Up to 40Km reach for G.652 SMF with FEC
- Duplex LC receptacle
- I-Temp range: -40 to 85°C
- Single 3.3V power supply
- RoHS 2.0 compliant (2011/65/EU, lead free)

Applications

- 25GBASE-ER Ethernet
- CPRI Operation1,2

Description

This product is a high-performance SFP28 transceiver module designed for optical communication, which is both compliant with IEEE 25GBASE-ER and CPRI option 10 standards. Its high performance cooled EML transmitter and high sensitivity APD receiver can provide superior performance for 25G application up to 30km/40km(with FEC) Links.

Note:

1. Can support CPRI-3/5/7 and CPRI option 10.
2. Please follow our guide to shift to CPRI operation as figure 3 shown.

Block Diagram

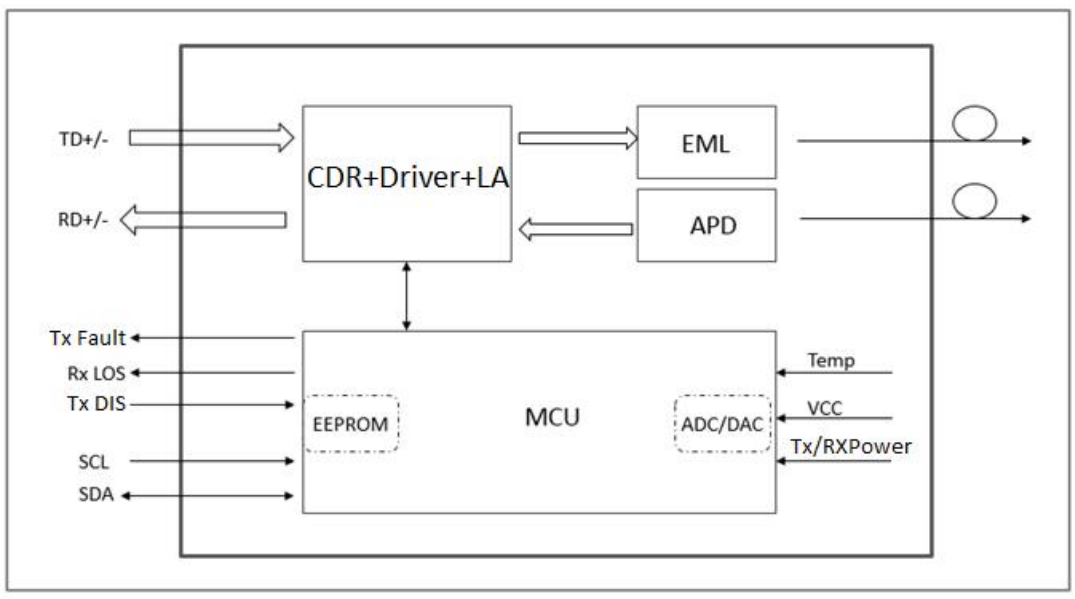

Figure 1. Module Block Diagram

The SFP28 is an enhanced Small Form Factor Pluggable SFP+ transceiver, and can be contacted through I2C system.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-40	85	°C
Case Operating Temperature	T_c	-40	85	°C
Humidity (non-condensing)	Rh	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	-40		85	°C
Data Rate Per Lane	fd		25.78		Gb/s
Humidity	Rh	0		85	%
Power Dissipation	P_m			2	W
Fiber Bend Radius	R_b	3			cm

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude	ΔV_{out}	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			5E-5	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Data Rate	BR		25.78		Gbps
Center Wavelength	λc1	1272.55		1274.54	nm
Center Wavelength	λc2	1276.89		1278.89 1278.8	nm
Center Wavelength	λc3	1281.25		1283.27	nm
Center Wavelength	λc4	1285.65		1287.69	nm

Parameter	Symbol	Min	Typical	Max	Unit
Center Wavelength	λc5	1290.07		1292.12	nm
Center Wavelength	λc6	1294.53		1296.59	nm
Center Wavelength	λc7	1299.02		1301.09	nm
Center Wavelength	λc8	1303.54		1305.63	nm
Center Wavelength	λc9	1308.09		1310.19	nm
Average Launch Power	P_{out}	-3		6	dBm
Optical Modulation Amplitude	OMA	0		6	dBm
Extinction Ratio	ER	7			dB
Average Launch Power of OFF Transmitter	P_{off}			-30	dB
$Rin_{20}OMA$				-130	dB/HZ
Optical return loss tolerance				20	dB
Receiver					
Center Wavelength	λ_C	1260		1600	nm
Receiver Sensitivity in OMA[3]				-19	dBm
Stressed Receiver Sensitivity in OMA[3]				-16.5	dBm
Average Power at Receiver Input (each lane)		-27		-5	dBm
Receiver Reflectance	R_R			-26	dB
LOS Assert	LOS_A	-30			dBm
LOS De-Assert – OMA	LOS_D			-17	dBm
LOS Hysteresis	LOS_H	0.5			dB

Note:

3. Hit Ratio = 5×10^{-5}

Pin Description

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	4
2	LVTTL-O	TX_Fault	Module Transmitter Fault	5
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	5
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	5
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select	
10		VeeR	Module Receiver Ground	4
11		VeeR	Module Receiver Ground	4
12	CML-O	RD-	Receiver Inverted Data Output	

Pin	Logic	Symbol	Name/Description	Note
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	4
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	4
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	4

Note:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

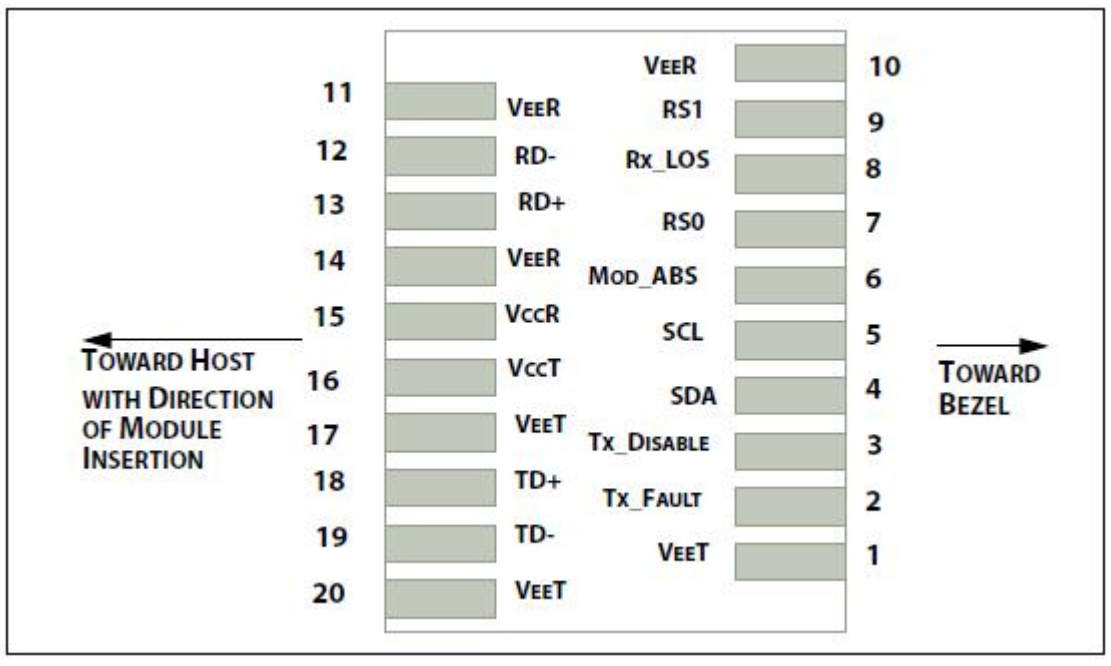

Figure 2. Electrical Pin-out Details

TX_FAULT Pin

Tx_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. The Tx_Fault output is an open drain/collector and shall be pulled up to the Vcc_Host in the host with a resistor in the range 4.7 kΩ to 10 kΩ.

TX_DISABLE Pin

When Tx_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off unless the module is a passive cable assembly. This contact shall be pulled up to VccT with a 4.7 kΩ to 10 kΩ resistor in modules and cable assemblies.Tx_Disable is a module input contact.

RS0/RS1 Pin

RS0 and RS1 are module inputs and are pulled low to VeeT with > 30 kΩ resistors in the module. RS0 optionally selects the optical receive signaling rate coverage. RS1 optionally selects the optical transmit signaling rate coverage.

Logic OR of RS0 and RS0 bit	Logic OR of RS1 and RS1 bit	RX CDR STATUS	TX CDR STATUS
High/1	High/1	Working	Working
High/1	Low/0	Bypass	Bypass
Low/0	High/1	Bypass	Bypass
Low/0	Low/0	Bypass	Bypass

Figure 3. CPRI Rate Shift Guide

MOD_ABS Pin

Mod_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this contact up to Vcc_Host with a resistor in the range 4.7 kΩ to10 kΩ.Mod_ABS is asserted "High" when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF-8074i) this contact has the same function but is called MOD_DEF0.

RX_LOS Pin

Rx_LOS when high indicates an optical signal level below that specified in the relevant standard. Rx_LOS is an open drain/collector output, but may also be used as an input by supervisory circuitry in the module. For a nominally 3.3 V Vcc_Host using a resistive pull up to Vcc_Host the resistor value shall be in the range 4.7 kΩ to 10 kΩ. For a nominally 2.5 V Vcc_Host using a resistive pull up to Vcc_Host the resistor value shall be in the range 4.7 kΩ to 7.2 kΩ.

Recommended Interface Circuit

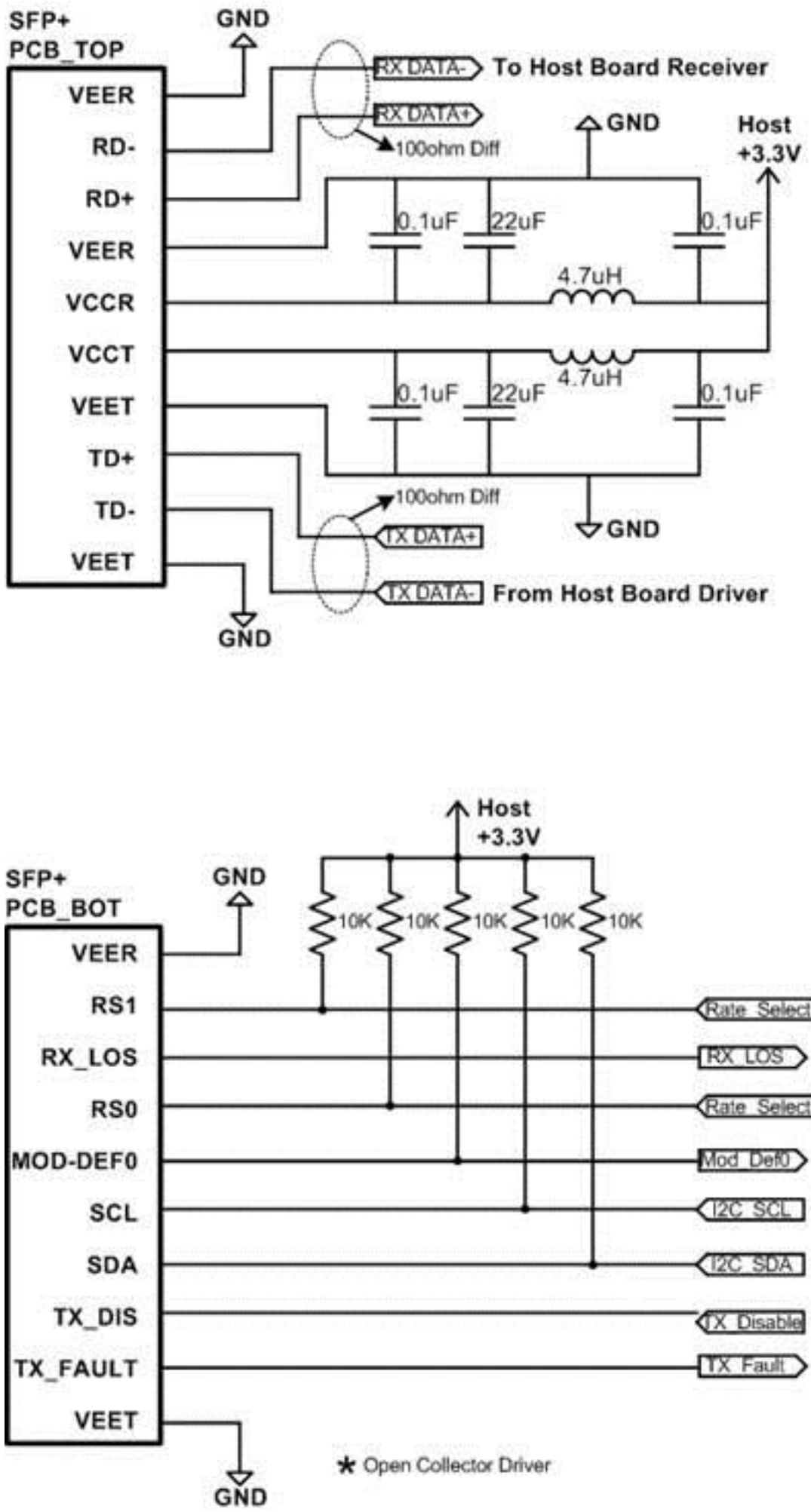

Figure 4. Recommended Interface Circuit

Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The memory map specific data field defines as following.

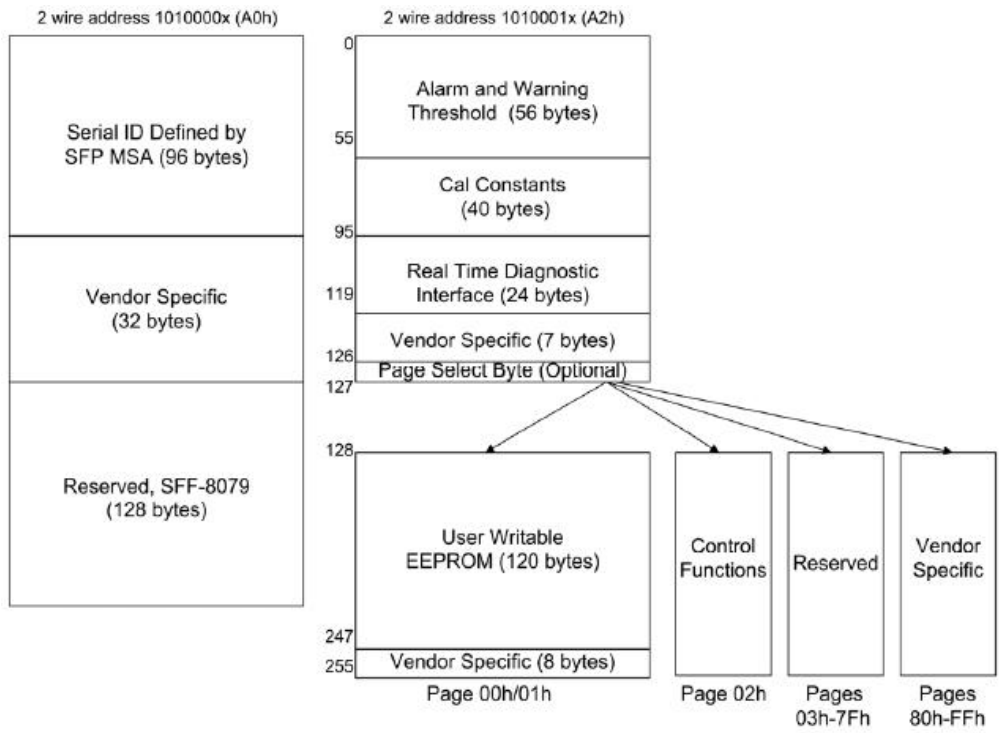

Figure 5. SFP28 Memory Map

Timing and Electrical

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Tx_Disable assert time	t_off		100	µs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		µs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

Figure 6. Timing Specification.

Mechanical Dimensions

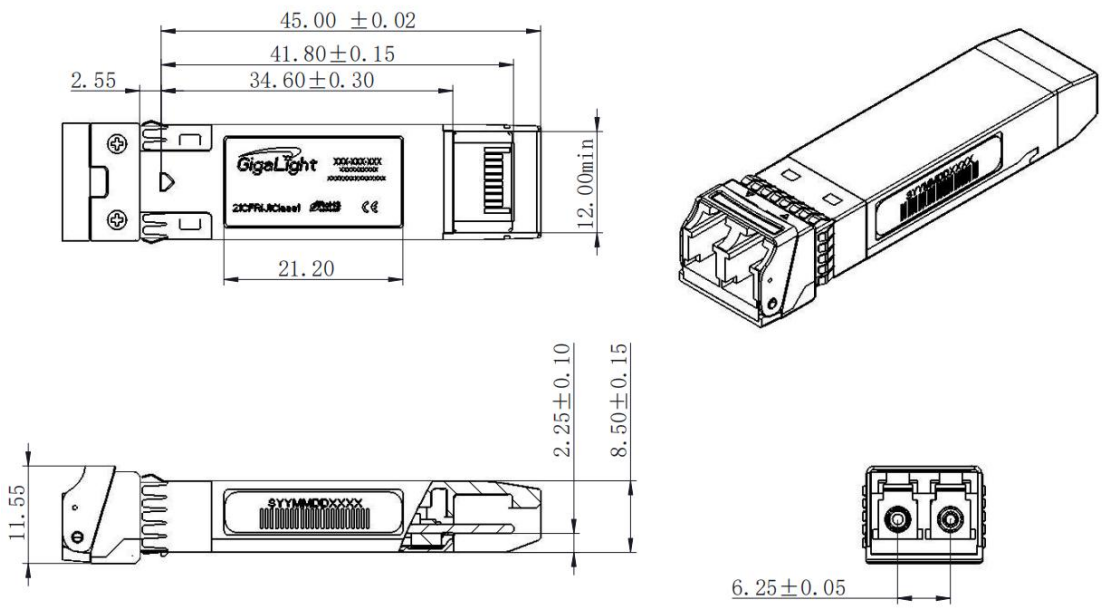

Figure 7. Mechanical Specifications

Regulatory Compliance

FIBERSTAMP[FBC-D25LxxK40T transceiver is Class 1 Laser Products. It is certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (Third Edition)
Environmental protection	2011/65/EU
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

References

1. SFP28 MSA

2. Ethernet IEEE802.3

3. CPRI standard

4. Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
FBC-D25LxxK40T	SFP28, EML, 25G Ethernet, CPRI, 30KM/40km, -40°C ~ +85°C
X (Wavelength ID.)	0=1273.55nm; 1=1277.89nm; 2=1282.26nm; 3=1286.66nm; 4=1291.10nm; 5=1295.56nm; 6=1300.05nm; 7=1304.58nm; 8=1309.14nm.

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