25Gbps 1310nm SFP28 Transceiver

FBC-D2531K10T

Features

- Hot-pluggable SFP28 form factor
- Supports 25Gbps data rate
- Maximum link length of 10km
- 1310nm DFB laser and PIN photo-detector
- Internal CDR on both Transmitter and Receiver channel
- Duplex LC receptacle
- Single 3.3V power supply
- Power dissipation < 1.5W
- Digital diagnostics functions are available via the I2C
- RoHS-6 compliant
- Commercial case temperature range: -40°C to 85°C

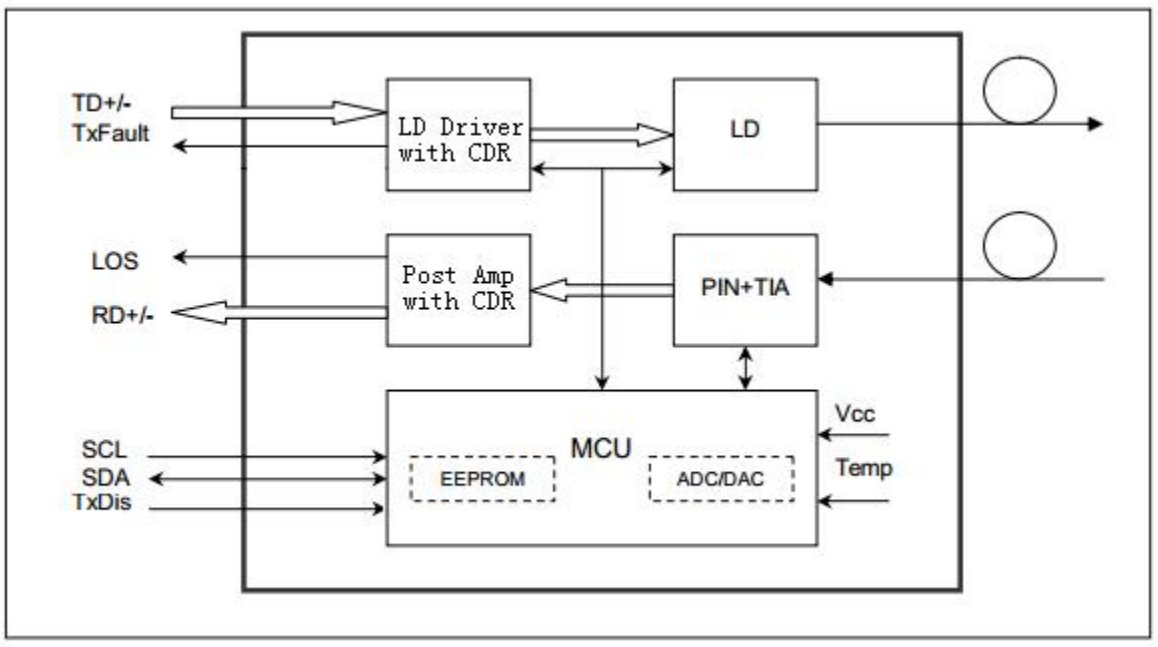
Applications

- 25GBASE-LR Ethernet

Description

The FIBERSTAMP Technologies FBC-D2531K10C is a single-Channel, Pluggable, Fiber-Optic SFP28 for 25 Gigabit Ethernet Applications. It is a high performance module for short-range data communication and interconnect applications which operate at 25.78125 Gbps up to 10km. This module is designed to operate over single mode fiber systems using a nominal wavelength of 1310nm. The electrical interface uses a 20 contact edge type connector. The optical interface uses duplex LC receptacle. This module incorporates FIBERSTAMP Technologies proven circuit and technology to provide reliable long life, high performance, and consistent service.

Block Diagram



Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	℃
Operating Humidity	-	5	85	%

Recommended Operating Conditions

Table2-Recommend Operating Conditions

Parameter		Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Commercial	Tc	-40		+85	℃
Power Supply Voltage		Vcc	3.13	3.3	3.47	V
Power Supply Current		Icc			450	mA

Optical and Electrical Characteristics

Table3- Optical and Electrical Characteristics

Parameter		Symbol	Min	Typical	Max	Unit	Notes
Transmitter							
Data rate		BR		25.78		Gbps	
Centre Wavelength		λc	1295	1310	1325	nm	
Spectral Width (-20dB)		σ			1	nm	
Side Mode Suppression Ratio		SMSR	30			dB	
Average Output Power		Pavg	-1.5		2	dBm	
Extinction Ratio		ER	3.5			dB	
Differential data input swing		$V_{IN,PP}$	180		700	mV	
Input Differential Impedance		Z_{IN}	90	100	110	Ω	
TX Disable	Disable		2.0		Vcc	V	
	Enable		0		0.8	V	
TX Fault	Fault		2.0		Vcc	V	
	Normal		0		0.8	V	
Receiver							
Data rate		BR		25.78		Gbps	
Centre Wavelength		λc	1295	1310	1325	nm	
Average Receive Power		Pavg	-13.3		2	dBm	
Unstressed Receiver Sensitivity (OMA)		Psens	-	-	-13.0	dBm	1
LOS De-Assert		LOS_D			-12	dBm	
LOS Assert		LOS_A			-13	dBm	
LOS Hysteresis			0.5			dB	

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential data output swing	Vout,PP	300		900	mV	
LOS	High	2.0		Vcc	V	
	Low			0.8	V	

Notes1: For 25G-LR with FEC, receiver sensitivity is defined at 5E-5 BER level, not 10-12 BER level.

Timing and Electrical

Table4-Timing and Electrical

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Tx_Disable assert time	t_off		100	µs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		µs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

Diagnostics

Table 5 – Diagnostics Specification

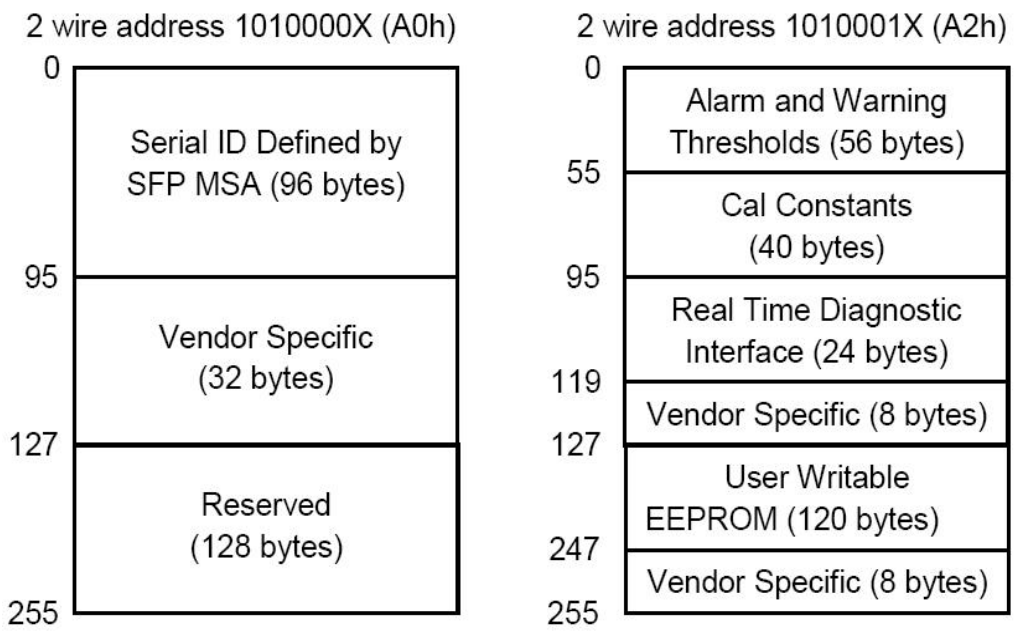
Parameter	Range	Unit	Accuracy	Calibration
Temperature	-40 to +85	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 100	mA	±10%	Internal / External
TX Power	-1.5 to 4.5	dBm	±3dB	Internal / External
RX Power	-14 to 4.5	dBm	±3dB	Internal / External

Digital Diagnostic Memory Map

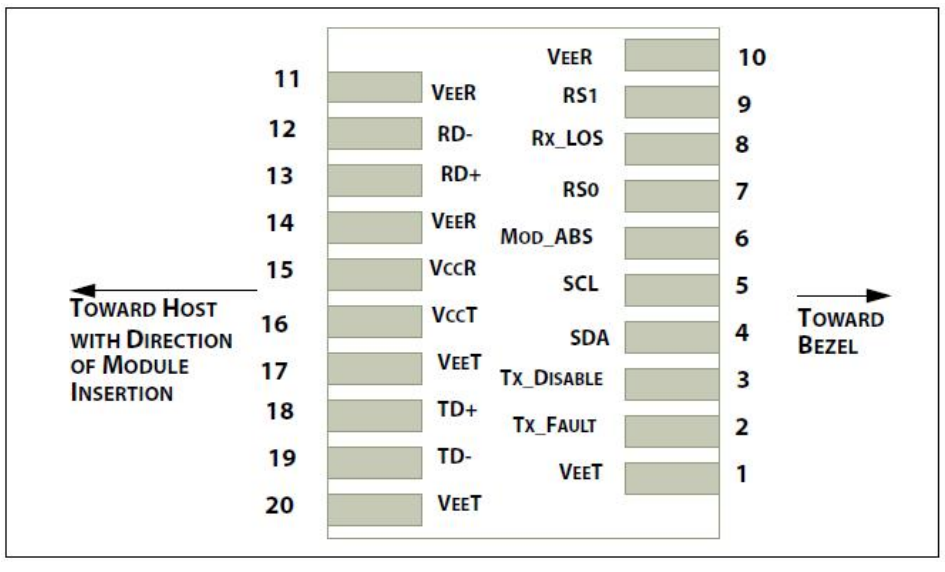
The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

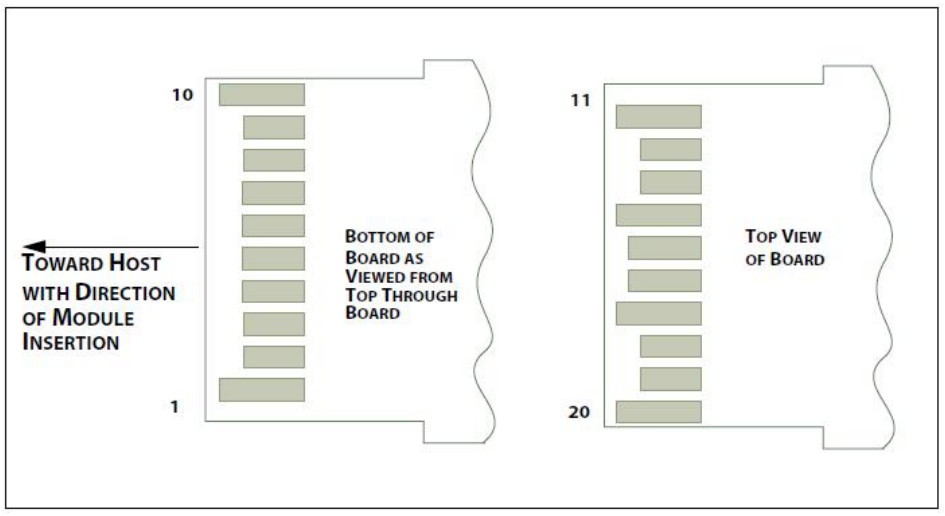
The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following.



Pin Definitions





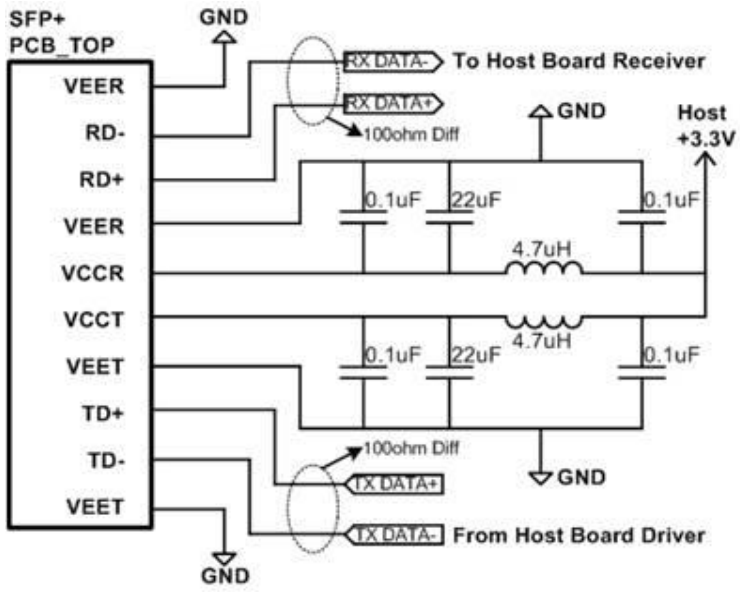
Pin Descriptions

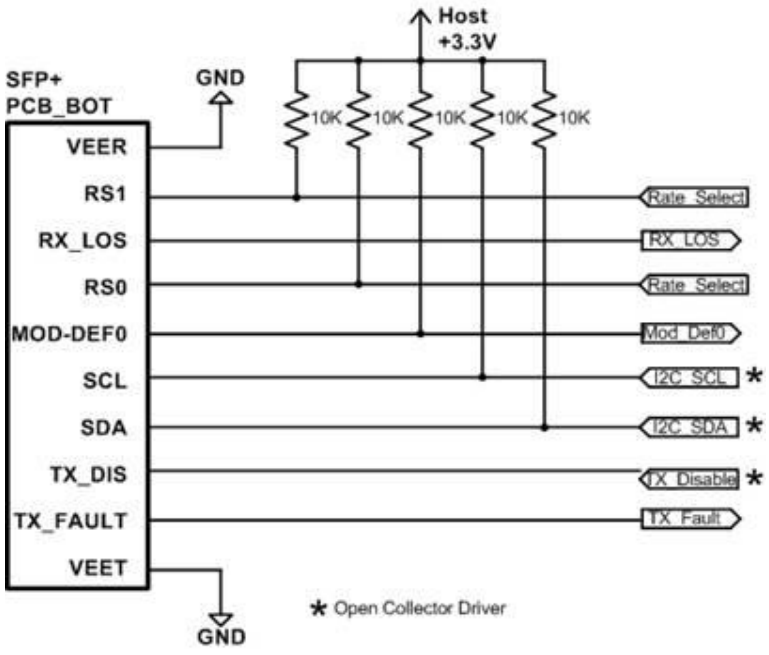
PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

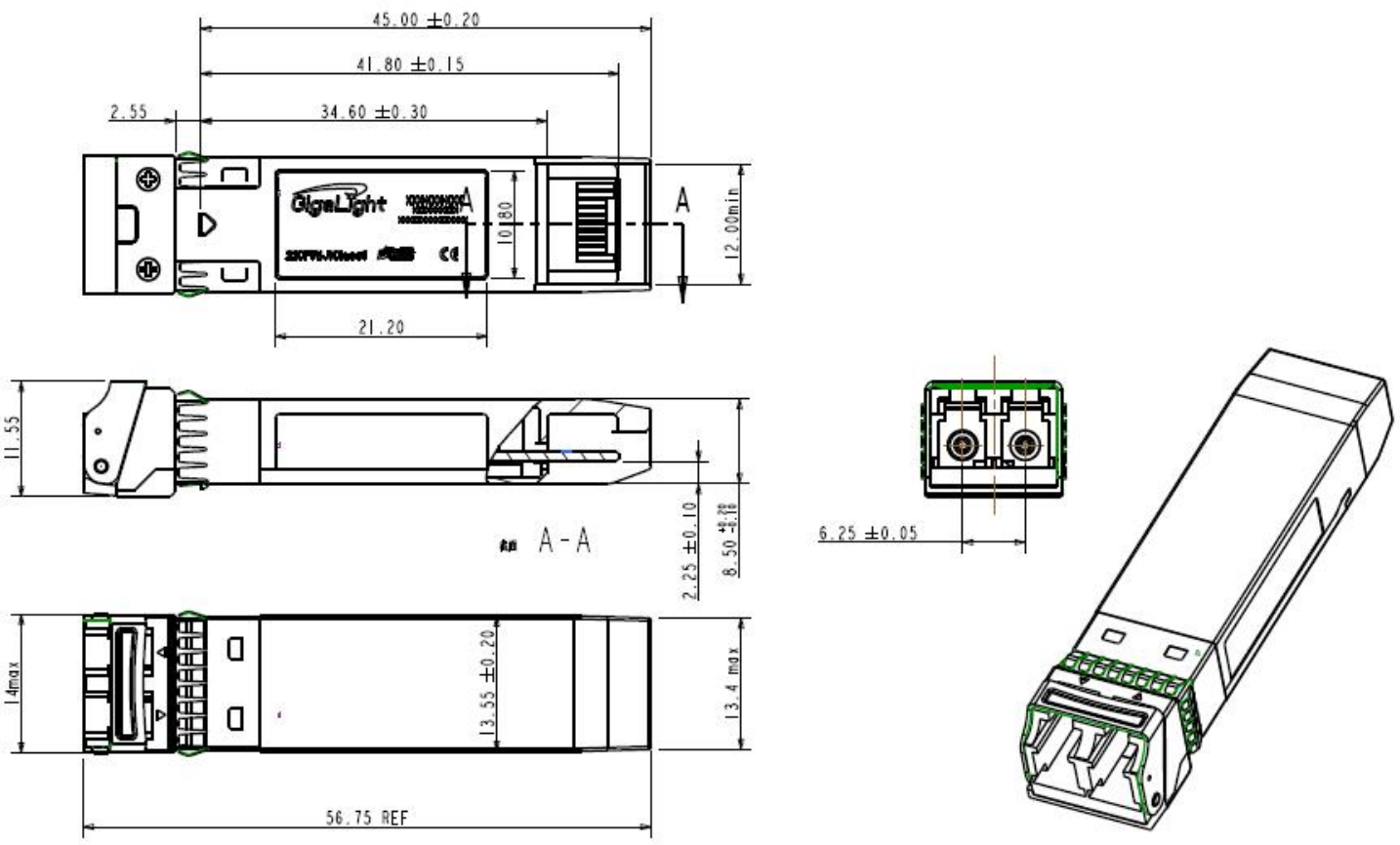
1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Interface Circuit





Mechanical Dimensions



Ordering information

Part Number	Product Description
FBC-D2531K10T	25Gbps, 1310nm; SFP28, 10km, DDM -40ºC ~ +85ºC

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