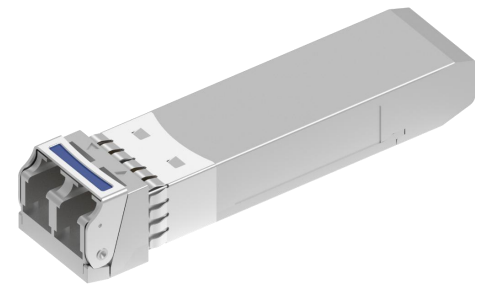


25Gbps 1310nm SFP28 Transceiver

FBC-D2531K10C

Features

- Hot-pluggable SFP28 form factor
- Supports 25Gbps data rate
- Maximum link length of 10km
- 1310nm DFB laser and PIN photo-detector
- Internal CDR on both Transmitter and Receiver channel
- Duplex LC receptacle
- Single 3.3V power supply
- Power dissipation < 1.0W
- RoHS 2.0 compliant (2011/65/EU, lead free)
- Commercial case temperature range: 0°C to 70°C



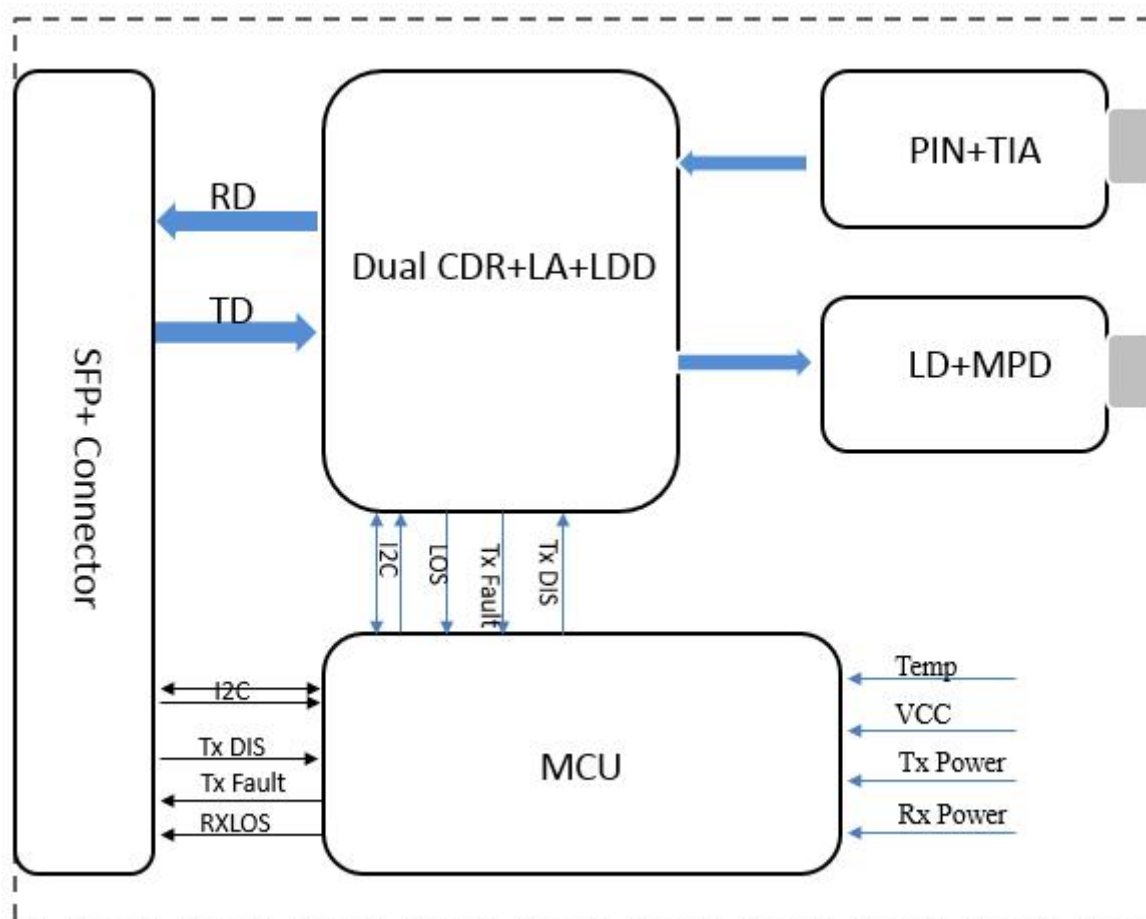
Applications

- 25GBASE-LR Ethernet

Description

The FIBERSTAMP Technologies FBC-D2531K10C is a single-Channel, Pluggable, Fiber-Optic SFP28 for 25 Gigabit Ethernet Applications. It is a high performance module for short-range data communication and interconnect applications which operate at 25.78125 Gbps up to 10km. This module is designed to operate over single mode fiber systems using a nominal wavelength of 1310nm. The electrical interface uses a 20 contact edge type connector. The optical interface uses duplex LC receptacle. This module incorporates FIBERSTAMP Technologies proven circuit and technology to provide reliable long life, high performance, and consistent service.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	-	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc			450	mA

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude1	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude2	ΔV_{out}	500		800	mVp-p
Input Logic Level High	V _{IH}	2.0		Vcc	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	Vcc-0.5		Vcc	V
Output Logic Level Low	V _{OL}	0		0.4	V

Note:

- 1、 Differential input voltage amplitude is measured between TxnP and TxnN.
- 2、 Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Data rate	BR		25.78		Gbps	
Centre Wavelength	λ_c	1295	1310	1325	nm	
Spectral Width (-20dB)	σ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Output Power	P _{avg}	-7		2	dBm	
Optical Modulation Amplitude	OMA	-4		2.2	dBm	
Extinction Ratio	ER	3			dB	
Eye Mask Coordinates		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				
Receiver						
Data rate	BR		25.78		Gbps	



Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	λ_c	1295	1310	1325	nm	
Average Power at Receiver		-13.3		2	dBm	
Receive reference(max)				-26	dB	
Receiver Sensitivity (OMA)	Psens	-	-	-12.0	dBm	1
Stressed receiver sensitivity(OMA)				-9.5	dBm	2
LOS De-Assert	LOSD			-12	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Hysteresis		0.5			dB	

Notes1:

- For 25G-LR with FEC, receiver sensitivity is defined at 5E-5 BER level, not 10-12 BER level.
- Measured with conformance test signal at TP3 for BER=5E-5.

Timing and Electrical

Parameter	Symbol	Min.	Max.	Unit	Conditions
Tx_Disable assert time	t_off		100	μ s	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		μ s	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	μ s	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	μ s	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	μ s	From occurrence of presence of signal to negation of Rx_LOS

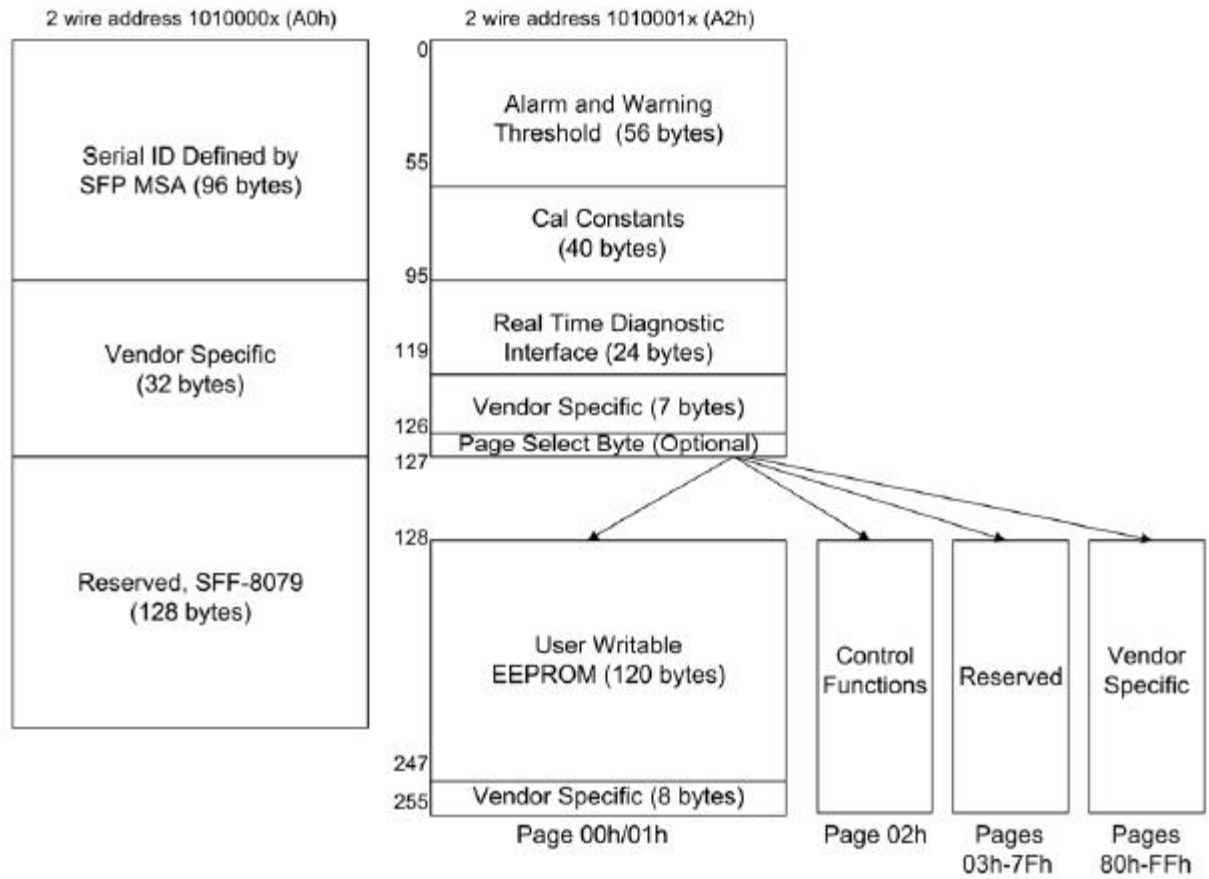
Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The memory map specific data field defines as following.

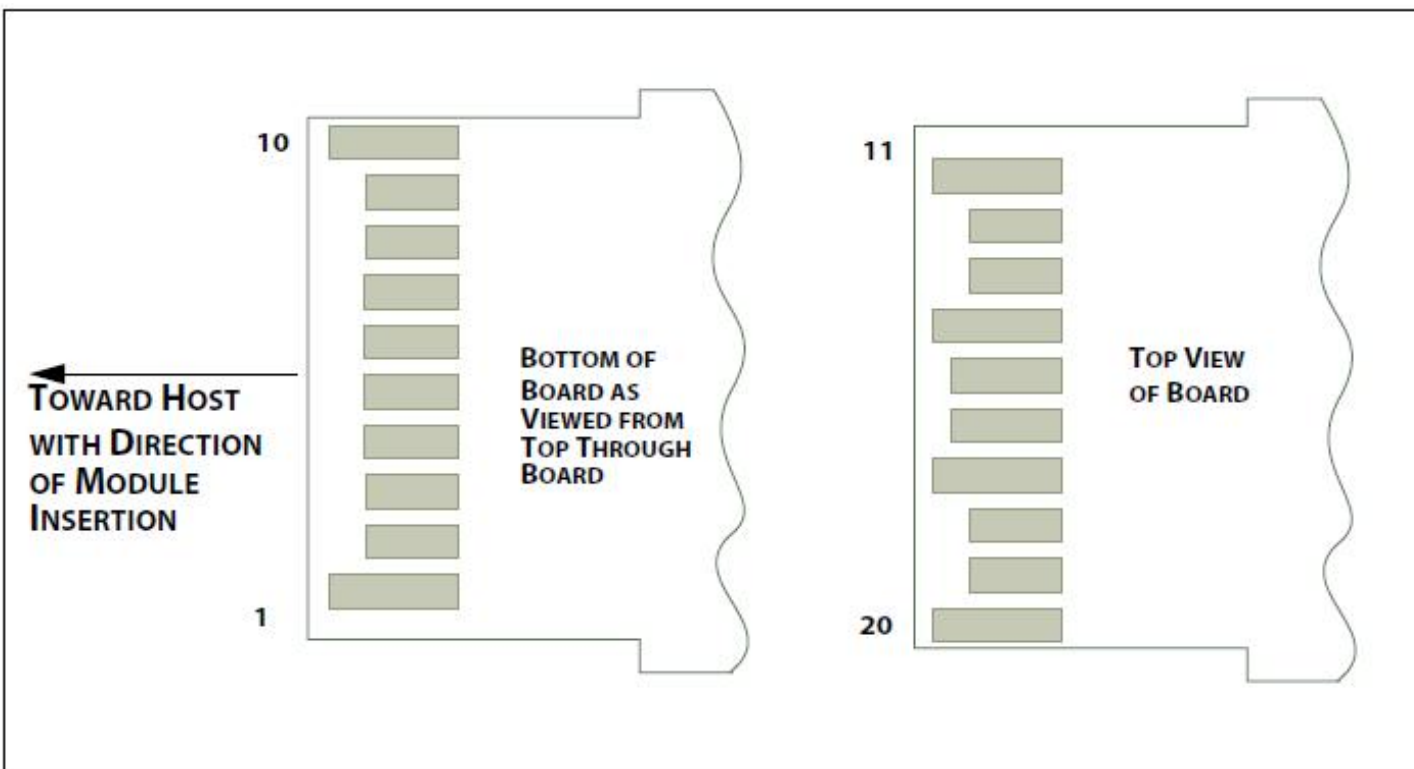
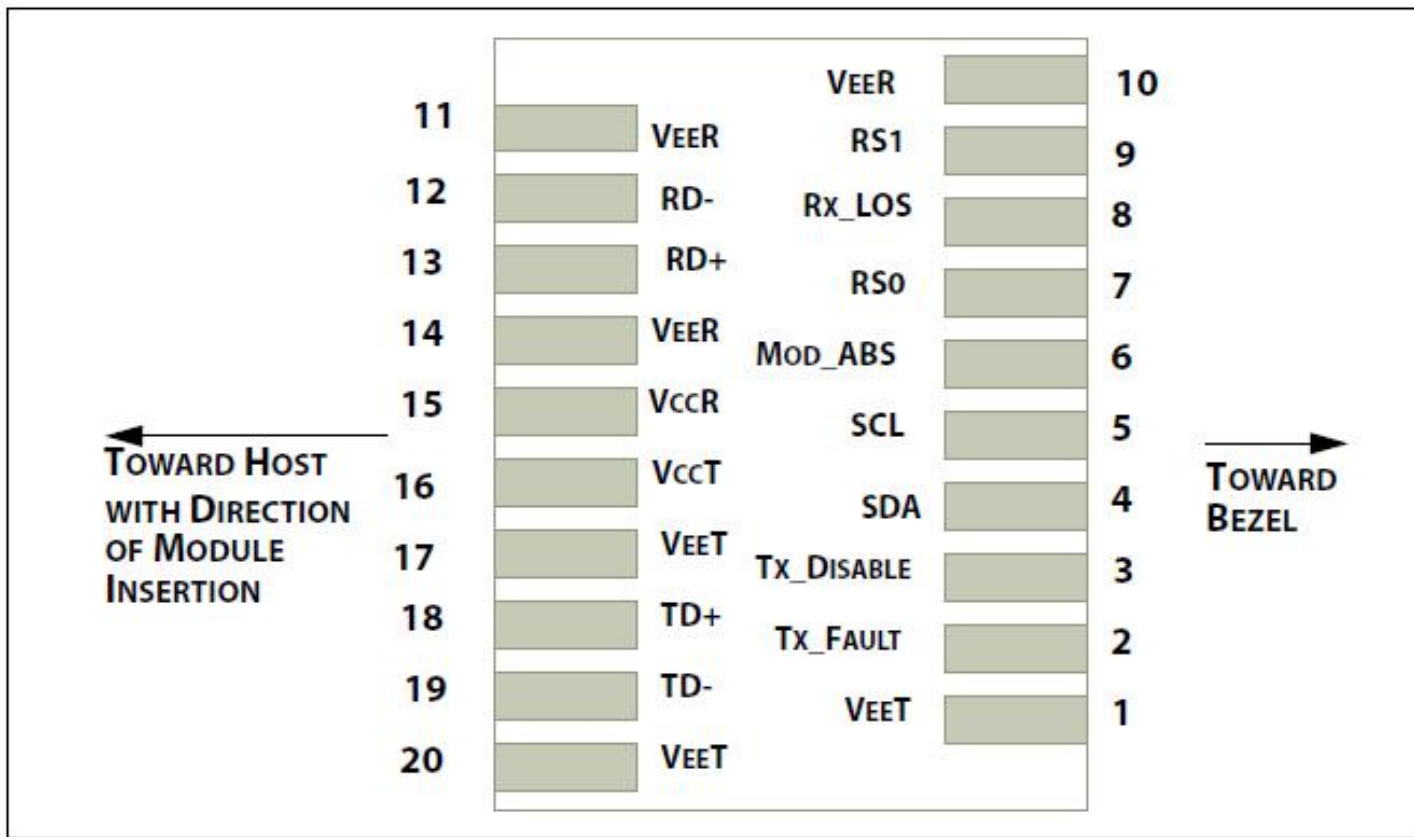


Two-wire Interface Fields



TWO-WIRE INTERFACE FIELDS

Pin Definitions



Pin Descriptions

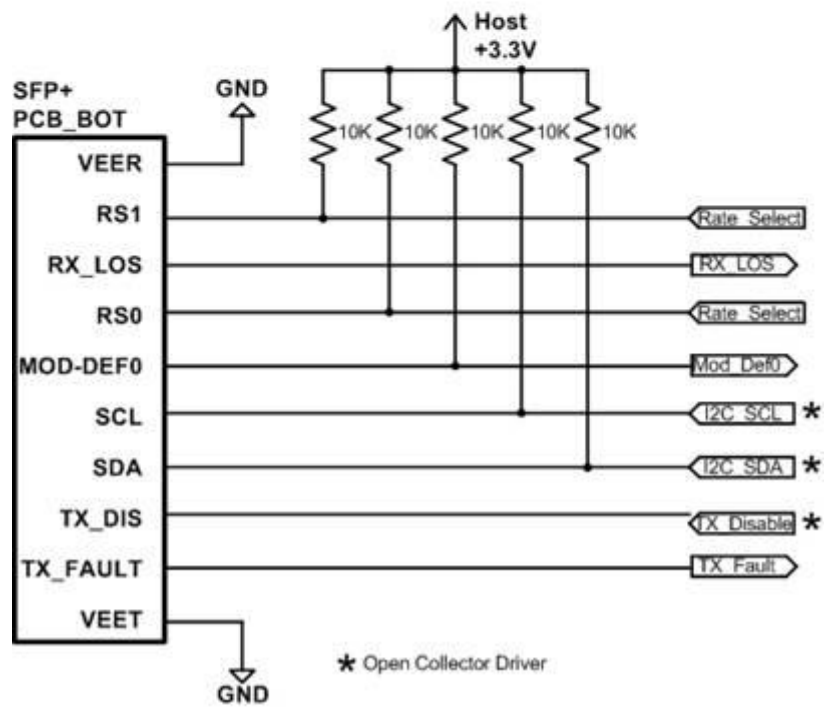
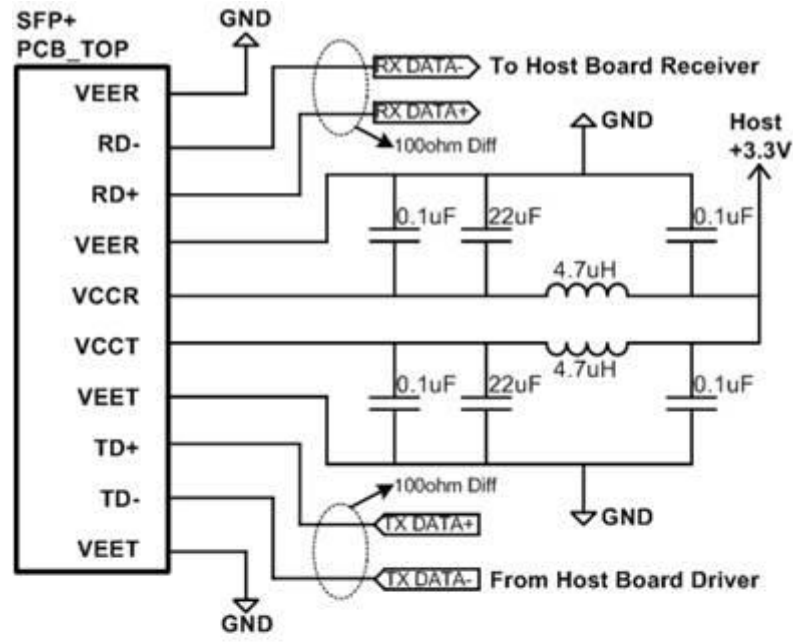
PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTTL-I	RS0	Receiver Rate Select	
8	LVTTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

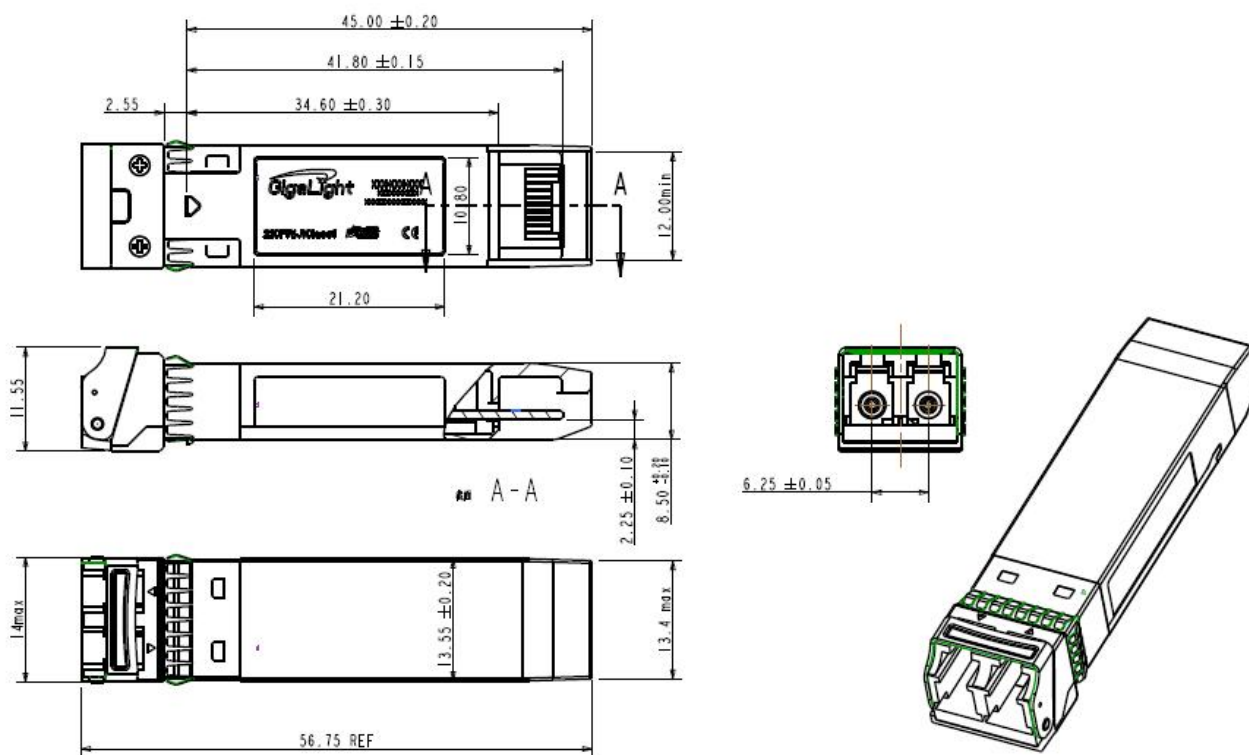
1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.



Recommended Interface Circuit



Mechanical Dimensions



Regulatory Compliance

FIBERSTAMP FBC-D2531K10C transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (Third Edition)
Environmental Protection	2011/65/EU
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

References

- SFP28 MSA
- Ethernet IEEE802.3cc
- Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.

CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FBC-D2531K10C	25Gbps, 1310nm; SFP28, 10km, 0°C ~ +70°C

Important Notice

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