

25Gbps SFP28 Bi-Directional Transceiver

FCC-D252733K10T

Features

- Hot-pluggable SFP28 form factor
- Up to 25Gbps data rate
- Maximum link length of 10km
- Single LC receptacle, Bi-directional
- CWDM DFB laser and PIN photo-detector
- 1270nm Tx/1330nm Rx
- Internal CDR on both Transmitter and Receiver channel
- Single 3.3V power supply
- Power dissipation < 1.6W
- RoHS 2.0 compliant (2011/65/EU, lead free) 
- Industrial case temperature range: -40°C to 85°C



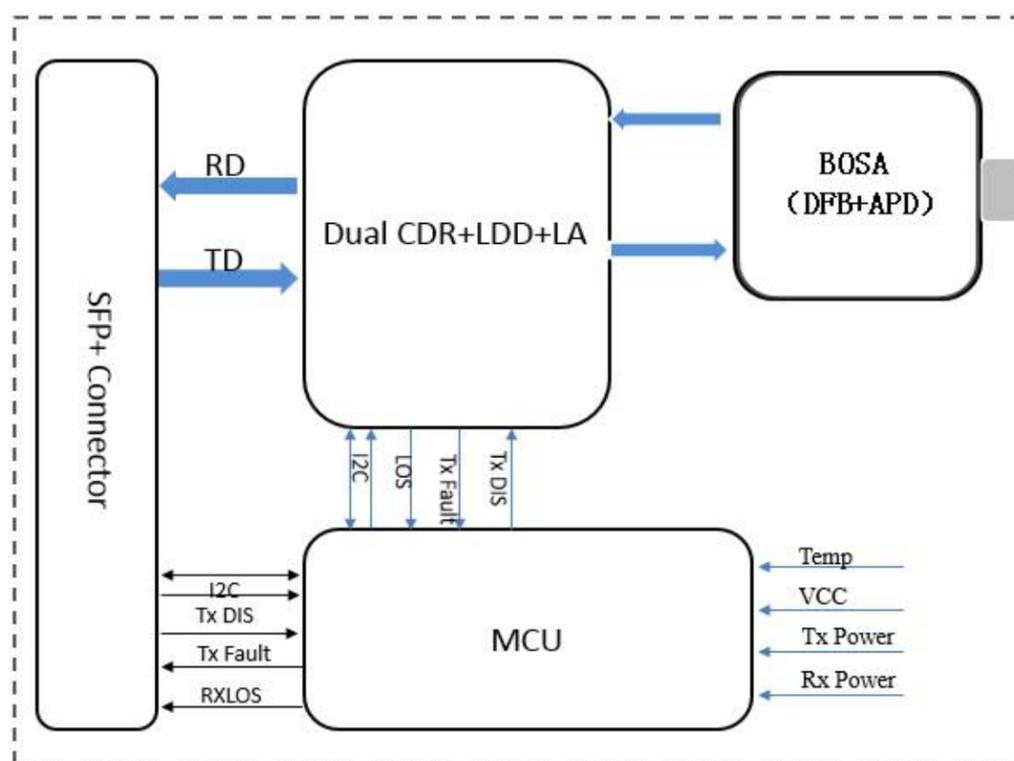
Applications

- 25G Ethernet
- CPRI Option 10
- Support 10G CPRI option 8 by CDR bypass

Description

The FIBERSTAMP Technologies FCC-D252733K10T is designed for Bi-directional 25G serial optical data communications by using 1270nm transmitter and 1330nm receiver. It is a high performance module for 25G Ethernet and Option 10 CPRI applications which operate up to 10km. This module incorporates FIBERSTAMP Technologies proven circuit and technology to provide reliable long life, high performance, and consistent service.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	-	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	-40		+85	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc			485	mA

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude1	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude2	ΔV_{out}	500		800	mVp-p
Input Logic Level High	V _{IH}	2.0		Vcc	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	Vcc-0.5		Vcc	V
Output Logic Level Low	V _{OL}	0		0.4	V

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Data rate	BR		25.78		Gbps	
Centre Wavelength	λ_c		1270		nm	
Spectral Width (-20dB)	σ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Output Power	P _{avg}	-2		6	dBm	
Optical Modulation Amplitude	OMA	-4		6	dBm	
Extinction Ratio	ER	3		6	dB	
Eye Mask Coordinates		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				
Receiver						
Data rate	BR		25.78		Gbps	

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	λ_c		1330		nm	
Average Power at Receiver				3	dBm	
Receive reflectance(max)				-26	dB	
Receiver Sensitivity (OMA)	P _{sens}	-	-	-12.0	dBm	1
LOS De-Assert	LOS _D			-12	dBm	2
LOS Assert	LOS _A	-30			dBm	
LOS Hysteresis		0.5			dB	

Notes:

- For 25G-LR with FEC, receiver sensitivity is defined at 5E-5 BER level, not 10-12 BER level.
- Measured with conformance test signal at TP3 for BER=5E-5.

Timing and Electrical

Parameter	Symbol	Min.	Max.	Unit	Conditions
Tx_Disable assert time	t _{off}		100	μs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t _{on}		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t _{2w_start_up}		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t _{start_up}		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t _{start_up_cooled}		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t _{power_level2}		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t _{power_down}		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t _{reset}	10		μs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t _{RS0_FC} , t _{RS1_FC}		500	μs	From assertion till stable output
RS0, RS1 rate select timing non FC	t _{RS0} , t _{RS1}		24	ms	From assertion till stable output
Rx_LOS assert delay	t _{los_on}		100	μs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t _{los_off}		100	μs	From occurrence of presence of signal to negation of Rx_LOS

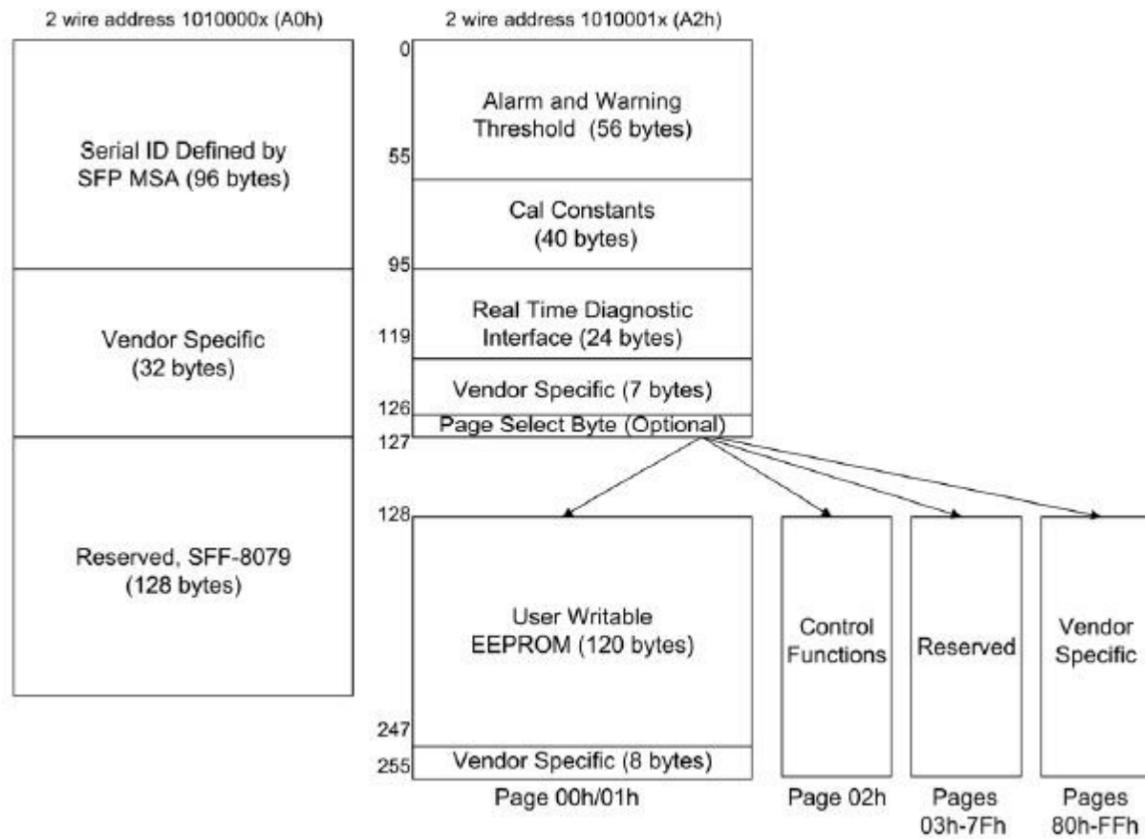
Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The memory map specific data field defines as following.



Two-wire Interface Fields



TWO-WIRE INTERFACE FIELDS

CDR Rate Select control

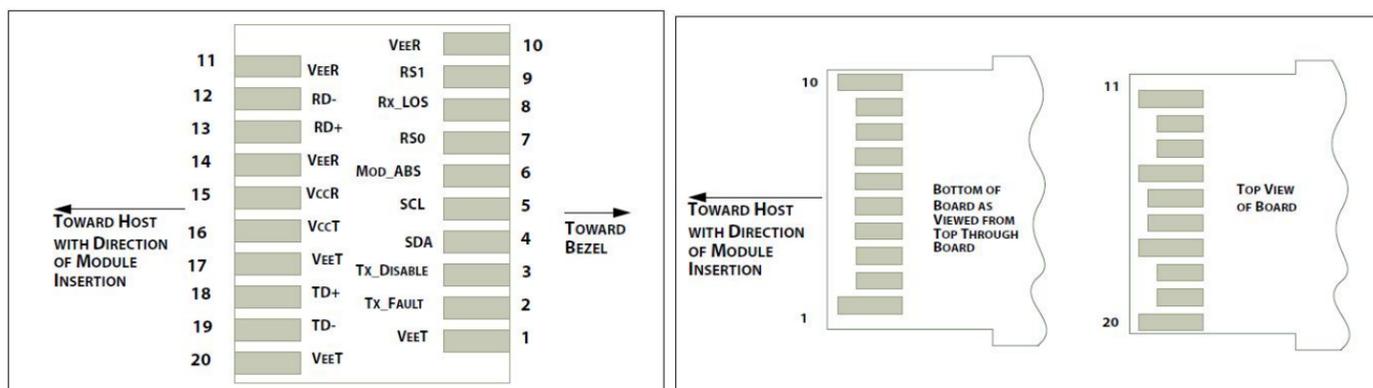
The soft RS(0) select bit(A2h byte 110 bit3) and soft RS(1) select bit(A2h byte118 bit3) are CDR control bits that allow for the CDR Rate Select using the 2-wire interface. These bits and the corresponding rate select pins RS0 and RS1 are connected through a logical OR function so that the CDR is controlled when either the bit is "1" or the pin is "high".

TABLE 10-2 RETIMER/CDR RATE SELECT LOGIC TABLE

When byte 13d of A0h is set to 0Eh and bit 64.3 of A0h is set to 1			
Logic OR of RS0 pin and RS0 bit	Logic OR of RS1 pin and RS1 bit	Receiver retimer/CDR	Transmitter retimer/CDR
Low/0	Low/0	Lock at low bit rate	Lock at low bit rate
Low/0	High/1	Lock at high bit rate	Bypass
High/1	Low/0	Bypass	Bypass
High/1	High/1	Lock at high bit rate	Lock at high bit rate

Note: Low and high bit rates are defined in byte 13d of A0h.

Pin Definitions



Pin Descriptions

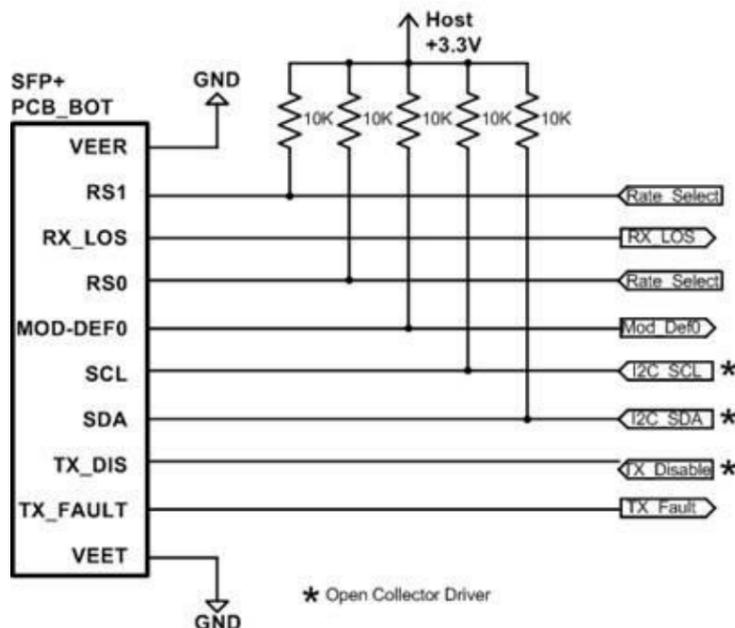
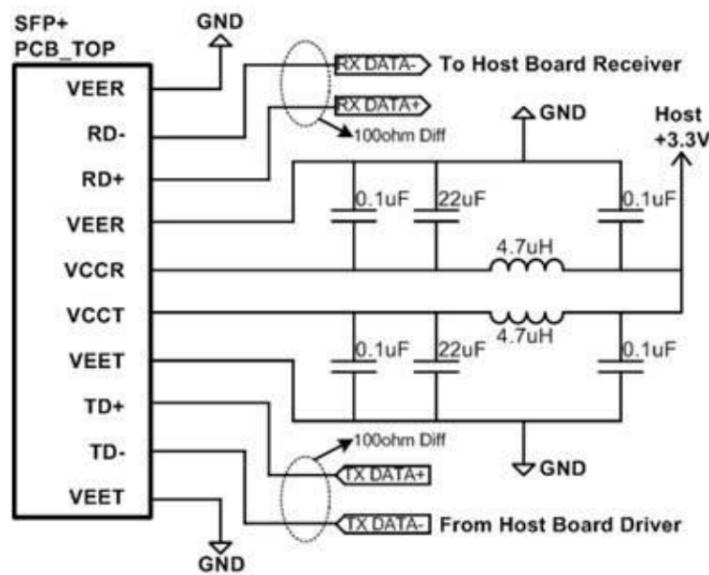
PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	

PIN	Logic	Symbol	Name / Description	Note
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

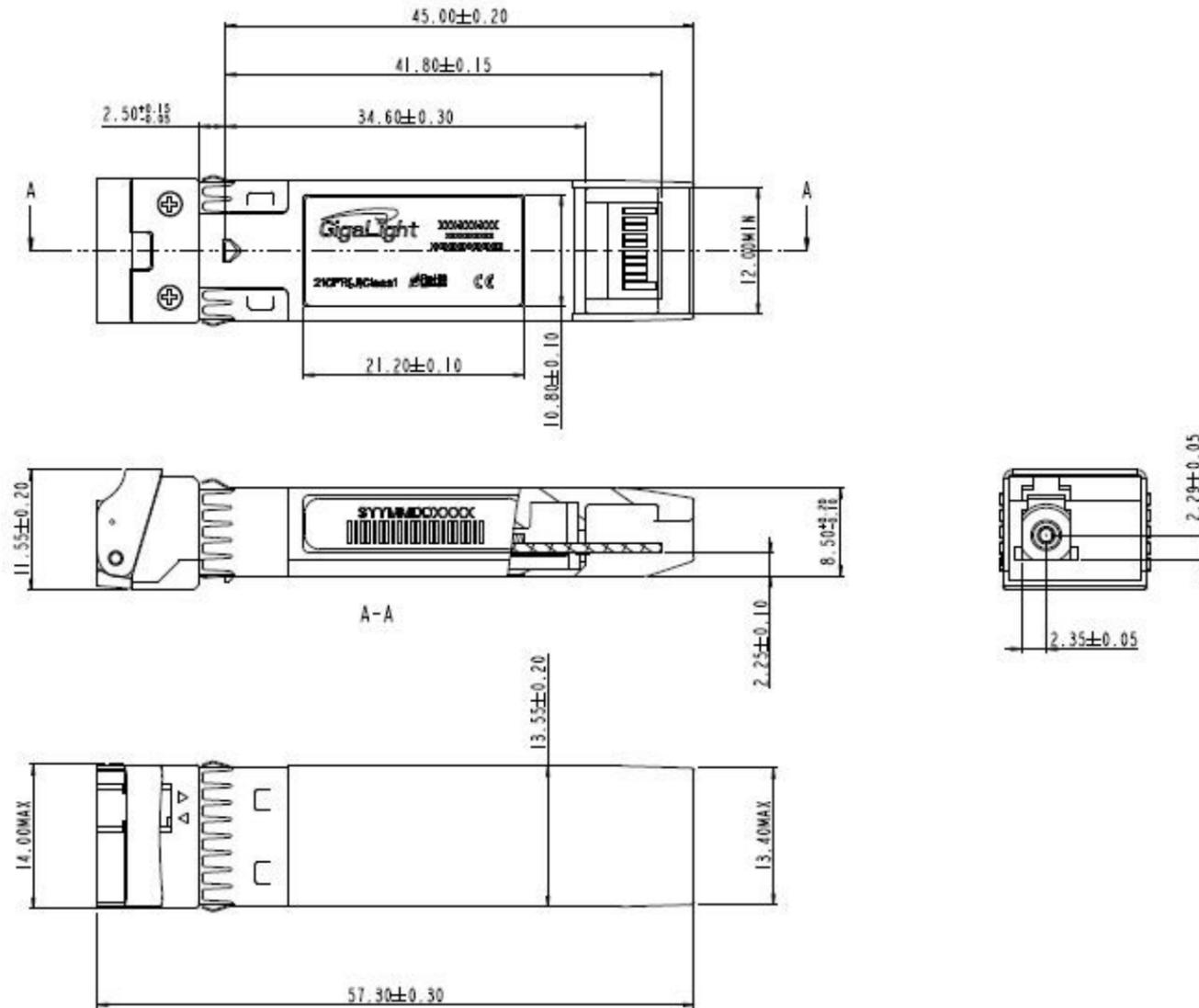
Notes:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Interface Circuit



Mechanical Dimensions



Regulatory Compliance

FIBERSTAMP FCC-D252733K20T transceivers are Class 1 Laser Products. They meet the requirements of the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3 rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

References

- SFP28 MSA
- Ethernet IEEE802.3cc
- Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.

 CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FCC-D252733K10T	25Gbps, 1270nm Tx/1330nm Rx; SFP28, 10km, -40°C ~ +85°C

Important Notice

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