200G QSFP-DD to 2XQSFP28 DAC

P/N: FWL-E25200XXC

Features

- ✓ Hot-plug QSFP-DD and QSFP28 form factor
- ✓ Support 8x 25Gb/s NRZ modulation
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ 26 AWG ~30 AWG support up to 5m length
- ✓ I2C management interface
- ✓ RoHS compliant

Applications

- ✓ Data storage and communication industry
- ✓ Switch / router / HBA
- ✓ Enterprise network
- ✓ SAN
- ✓ Data Center Network

STANDARDS COMPLIANCE

- IEEE802.3bj
- QSFP/QSFP-DD MSA

Description

FIBERSTAMP's FWL-E25200XXC cable assembly is a customized passive copper cable. The cable connects data signals from each of the 16 pairs on the single QSFP-DD end to the dual QSFP28 end, the 16 pairs operates at data rates of up to 25Gb/s, each end can be addressed by EEPROM to provide product information, which can be read or write by I2C interface.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_s	-20	85	°C
Case Operating	T_C	0	70	°C
Humidity	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case	T_C	0		70	°C
Baud Rate per Lane	fd		25.78		Gb/s
Humidity	Rh	5		85	%

High Speed Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance(bulk cable)	Rin1,P-P	95	100	110	Ω	
Differential Impedance (Mated connector)	Rin2,P-P	90	100	110	Ω	
Differential Impedance(cable termination)	Rin3,P-P	85	100	110	Ω	
Insertion loss	SDD21			22.48	dB	At 12.8906 GHz
Differential Return Loss	SDD11			See 1	dB	At 0.05 to 4.1 GHz

	SDD22			See 2	dB	At 4.1 to 19 GHz
Common-mode to common-mode output return loss	SCC11	2			dB	At 0.2 to 19 GHz
	SCC22					
Differential to common-mode return loss	SCD11			See 3	dB	At 0.01 to 12.89 GHz
	SCD22			See 4		At 12.89 to 19 GHz
Differential to common Mode Conversion Loss	SCD21			10	dB	At 0.01 to 12.89 GHz
				See 5		At 12.89 to 15.7 GHz
				6.3		At 15.7 to 19 GHz
Channel Operating Margin	COM	3			dB	

Notes:

1. Reflection Coefficient given by equation SDD11(dB) < 16.5 - 2 × SQRT(f), with f in GHz
2. Reflection Coefficient given by equation SDD11(dB) < 10.66 - 14 × log10(f/5.5), with f in GHz
3. Reflection Coefficient given by equation SCD11(dB) < 22 - (20/25.78)*f, with f in GHz
4. Reflection Coefficient given by equation SCD11(dB) < 15 - (6/25.78)*f, with f in GHz
5. Reflection Coefficient given by equation SCD21(dB) < 27 - (29/22)*f, with f in GHz

QSFP-DD end Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[Note5]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground [Note5]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[Note5]
8	LVTTL-I	MODSEIL	Module Select[Note6]
9	LVTTL-I	ResetL	Module Reset[Note6]
10		VCCRx	+3.3V Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[Note6]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[Note6]
13		GND	Module Ground[Note5]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[Note5]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[Note5]
20		GND	Module Ground[Note5]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[Note5]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[Note5]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[Note6]
32		GND	Module Ground[Note5]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[Note5]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[Note5]
39		GND	Module Ground[Note5]
40	CML-I	Tx6-	Transmitter inverted data input
41	CML-I	Tx6+	Transmitter non-inverted data input
42		GND	Module Ground [Note5]
43	CML-I	Tx8-	Transmitter inverted data input
44	CML-I	Tx8+	Transmitter non-inverted data input
45		GND	Module Ground[Note5]
46		Reserved	
47		TBD	For future use

48		VCC	+3.3V Receiver Power Supply
49		TBD	For future use
50		TBD	For future use
51		GND	Module Ground[Note5]
52	CML-O	RX7+	Receiver non-inverted data output
53	CML-O	RX7-	Receiver inverted data output
54		GND	Module Ground[Note5]
55	CML-O	RX5+	Receiver non-inverted data output
56	CML-O	RX5-	Receiver inverted data output
57		GND	Module Ground[Note5]
58		GND	Module Ground[Note5]
59	CML-O	RX6-	Receiver inverted data output
60	CML-O	RX6+	Receiver non-inverted data output
61		GND	Module Ground[Note5]
62	CML-O	RX8-	Receiver inverted data output
63	CML-O	RX8+	Receiver non-inverted data output
64		GND	Module Ground[Note5]
65		NC	No connect
66		TBD	For future use
67		VCC	+3.3V Power Supply
68		VCC	+3.3V Power Supply
69		TBD	For future use
70		GND	Module Ground[Note5]
71	CML-I	Tx7+	Transmitter non-inverted data input
72	CML-I	Tx7-	Transmitter inverted data input
73		GND	Module Ground[Note5]
74	CML-I	Tx5+	Transmitter non-inverted data input
75	CML-I	Tx5-	Transmitter inverted data input
76		GND	Module Ground[Note5]

Note:

Note5. Module circuit ground is isolated from module chassis ground within the module.

Note6. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

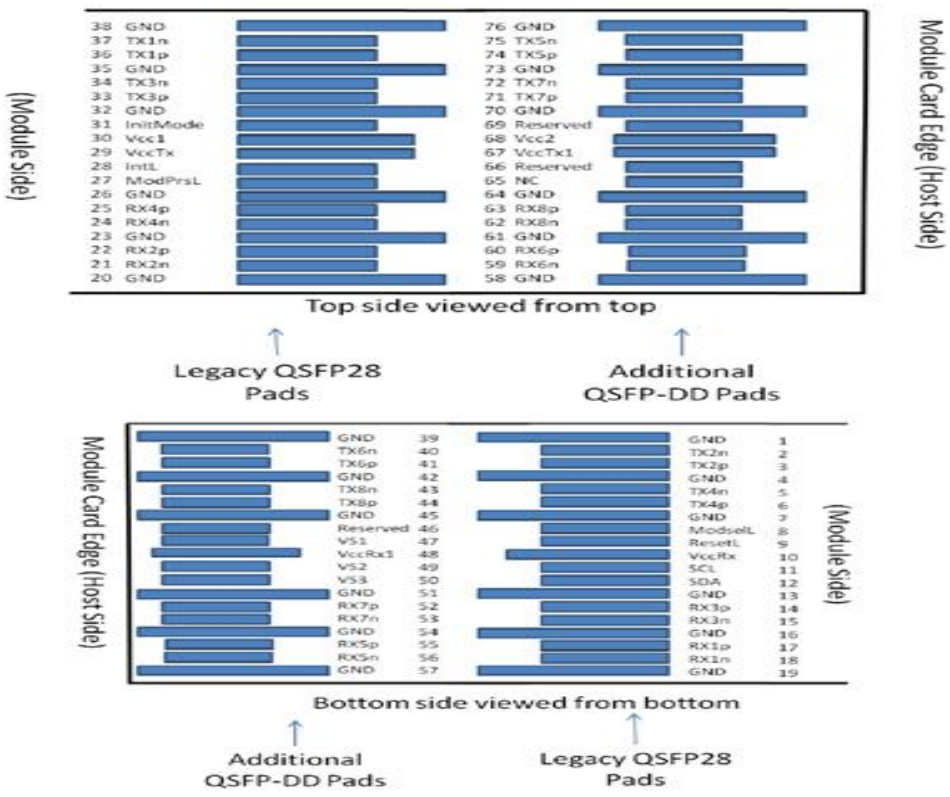


Figure 1. QSFP-DD Electrical Pin-out Details

QSFP28 end Pin Descriptions

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOSI/O	SCL	2-wire serial interface clock	
12	LVCMOSI/O	SDA	2-wire serial interface data	

13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Mechanical Dimensions

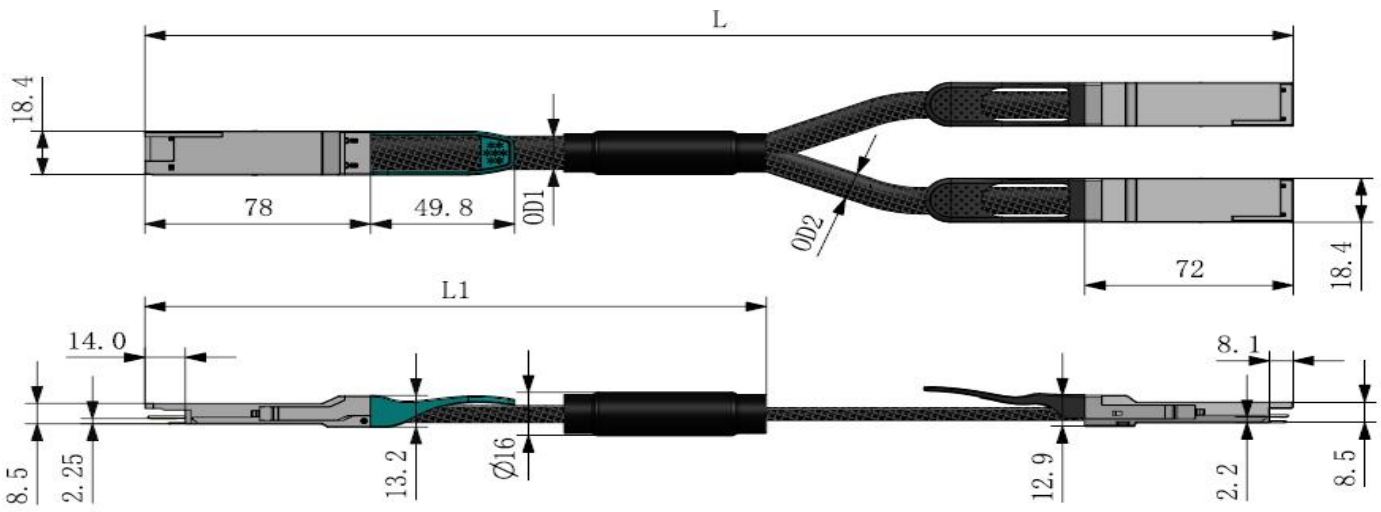
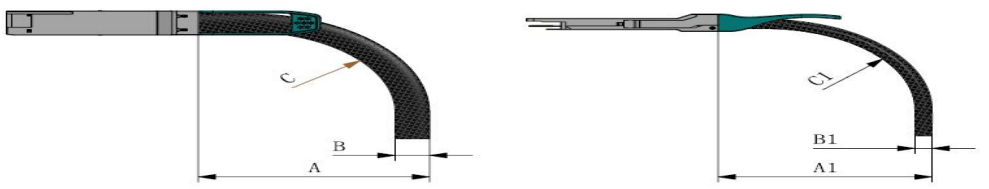


Figure 2. Typical Mechanical Specifications

QSFP Horizontal Direction			
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"
30AWG 8P	7.0MM	35MM	52MM
26AWG 8P	10MM	50MM	72MM

QSFP Vertical Direction			
CABLE GUAGE	DIAMETER"B1"	MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"
30AWG 8P	7.0MM	35MM	52MM
26AWG 8P	10MM	50MM	72MM



QSFP-DD Horizontal Direction			
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"
30AWG	10MM	50MM	70MM
26AWG	11MM	55MM	76MM
QSFP-DD Vertical Direction			
CABLE GUAGE	DIAMETER"B1"	MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"
30AWG	7MM	35MM	52MM
26AWG	9MM	45MM	64MM

Figure 3. Typical diameter and bend radius

Wiring connection diagram

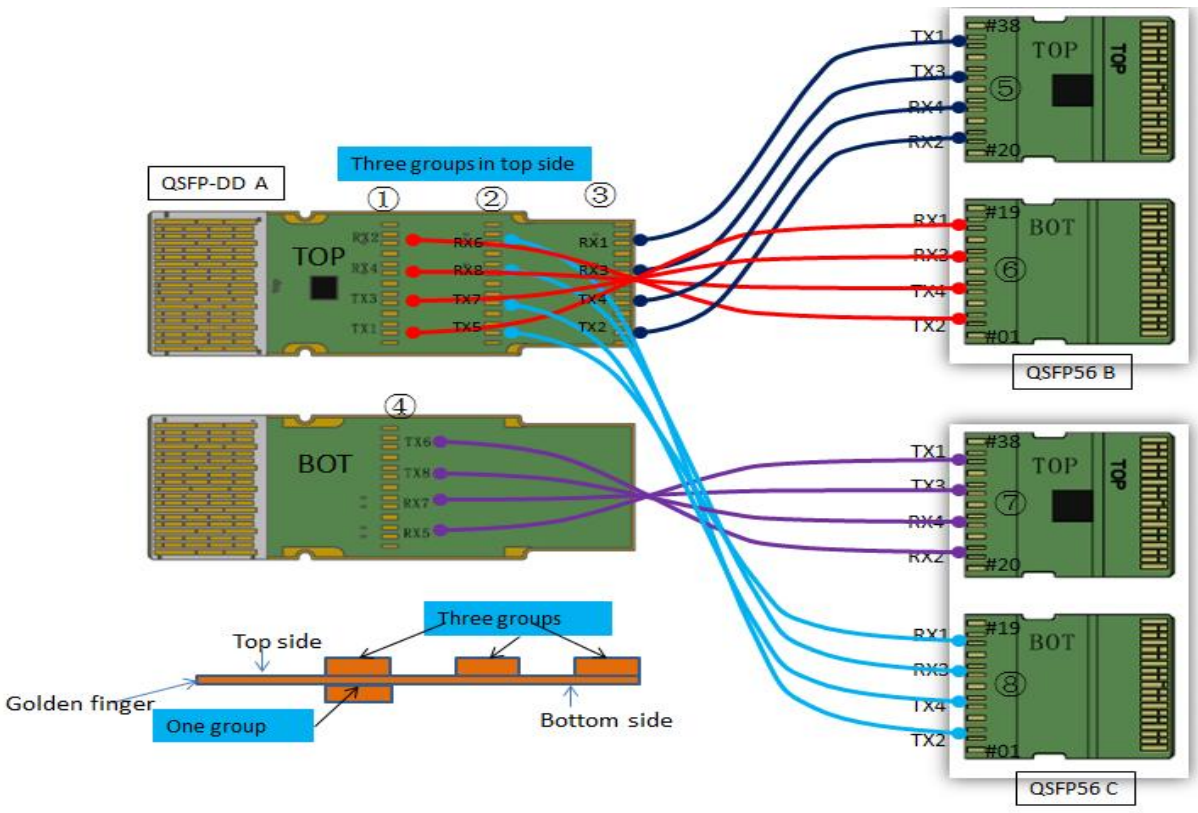


Figure 4. Wiring connection diagram

ENVIRONMENTAL

Item	Specificatio n
Physical shock	Subject mated specimens to 30G's half-sine shock pulses of 11 milliseconds duration. 3 shocks in each direction applied along 3 mutually perpendicular planes, 18 total shocks

Vibration (random)	Subject mated specimens to 3.10G's rms between 20-500 Hz for 15 minutes in each of 3 mutually
Thermal shock	100 cycles of: a) -55°C for 30 minutes b) +85°C for 30 minutes
Temperature Life	Subject mated Specimens to +105°C for 500 hours
Humidity and Temperature cycling	Subject unmated specimens to 10 cycles (10 days) between 25 and 65℃ at 80% to 100% RH
Visual Examination.	Connectors & contacts shall have no evidence of physical defects or otherwise unfit for testing.

Ordering information

Part Number	FWL-E25200XXC				
Length（meter）	1	2	3	4	5
Wire gauge（AWG）	30	30	26/30	26	26

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by FIBERSTAMP before they become applicable to any particular order or contract. In accordance with the FIBERSTAMP policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of FIBERSTAMP or others. Further details are available from any FIBERSTAMP sales representative.

E-mail: sales@fiberstamp.com
Official Site: www.fiberstamp.com

Revision History

Revision	Date	Description
V0	July-15-2025	Advance Release.