



200G QSFP DD PSM8 2km Optical Transceiver

FEL-200P8K02C

Features

- 8 channels full-duplex transceiver modules
- Supports 8×25Gb/s aggregate bit rates
- Supports 8×10Gb/s aggregate bit rates if required
- 8 channels 1310nm DFB
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <6W
- Hot Pluggable QSFP DD form factor
- Up to 2km reach for G.652 SMF
- Single male MPO(APC 8-degree) connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 2.0 compliant (lead free)

Applications

- 2×100G Ethernet links
- Infiniband DDR/EDR
- Datacenter and Enterprise networking

Description

The FIBERSTAMP Technologies FEL-200P8K02C is a Eight-Channel, Pluggable, Parallel, Fiber-Optic QSFP DD PSM8 for 2×100 Gigabit Ethernet, Infiniband DDR/EDR Applications. This transceiver is a high performance module for data communication and interconnect applications. It integrates eight data lanes in each direction with 208 Gbps bandwidth. Each lane can operate at 26Gbps up to 2km over G.652 SMF. These modules are designed to operate over singlemode fiber systems using a nominal wavelength of 1310nm. The electrical interface uses a 76 contact edge type connector. The optical interface uses an 24 fiber MTP (MPO) connector. This module incorporates FIBERSTAMP Technologies proven circuit and Optical technology to provide reliable long life, high performance, and consistent service.

200G QSFP DD PSM8 8CH CDR+ DRIVER 8CH DFB MPO MPO 8CH TIA+ CDR

Figure 1. Module Block Diagram

The 200Gb/s QSFP DD PSM8 is one kind of parallel transceiver. DFB and PIN array package is key technique, through I2C system can contact with module.







Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Тс	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Тс	0		70	°C
Data Rate Per Lane	fd	10.3125	25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		5.28	6	W
Fiber Bend Radius	Rb	0.002		2	km

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude1	ΔVin	190		700	mVp-p
Differential Output Voltage Amplitude2	ΔVout	300		850	mVp-p
Input Logic Level High	VIH	2.0		Vcc	V
Input Logic Level Low	VIL	0		0.8	٧
Output Logic Level High	VOH	Vcc-0.5		Vcc	٧
Output Logic Level Low	VOL	0		0.4	V

Note:

Differential input voltage amplitude is measured between TxnP and TxnN.

Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit		
Transmitter							
Center Wavelength	λс	1295	1310	1325	nm		
Side Mode Suppression Ratio	SMSR	30	-		dB		
Average Launch Power (each lane)	PAVG	-6	-	2	dBm		
Optical Modulation Amplitude (each lane)	РОМА	-5.0		2.2	dBm		
TDP,each lane	TDP			2.9	dB		





Parameter	Symbol	Min	Typical	Max	Unit	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Average Launch Power of OFF Transmitter (each lane)	POFF			-30	dB	
Eye Mask Coordinates1: X1, X2, X3, Y1, Y2, Y3 {0.31,0.4,0.45,0.34,0				Hit Ratio = 5x10-5		
R	eceiver					
Center Wavelength	λс	1295	1310	1325	nm	
Damage Threshold,each lane	THd	3.0			dBm	
Average Receive Power, each lane		-12.66		2.0	dBm	
Receive power, each lane (OMA) (max)				2.2	dBm	
Receiver Reflectance	RR			-26	dBm	
Receiver Sensitivity (OMA), each lane	SEN			-11.35	dBm	
LOS Assert	LOSA		-18		dBm	
LOS De-Assert – OMA	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5		3	dB	

Note:

Even if the TDP<1dB, the OMA min must exceed the minimum value specified here.

The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power. Sensitivity is specified at $5x10^{-5}$ BER at 25.78125Gb/s.

Pin Description

Table	1-	Pad	F	unction	Definition	1
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Pad	Logic	Symbol	Description	Plug	Notes
			10	Sequence4	
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	TALLT-I	ModSelL	Module Select	3B	
9	TALLT-I	ResetL	Module Reset	3B	0
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rж3р	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	0
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	:
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-0	ModPrsL	Module Present	3B	
28	LVTTL-0	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	тжЗр	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	4
	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
37	CME				





Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45	5-2-00	GND	Ground	1A	1
46	-	Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRxl	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50	e e	VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	1227
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54	:	GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	X.
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	500
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61	:	GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67	8	VccTx1	3.3V Power Supply	2A	2
68	:	Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	5
76	Company Cotto	GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vccl, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

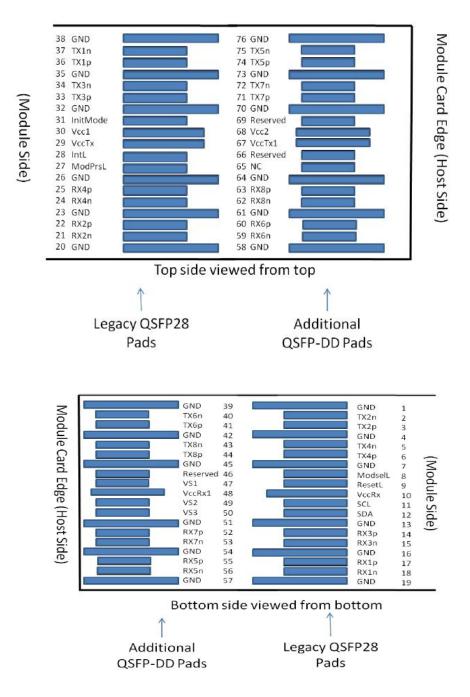


Figure 2. Electrical Pin-out Details





ModSell Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

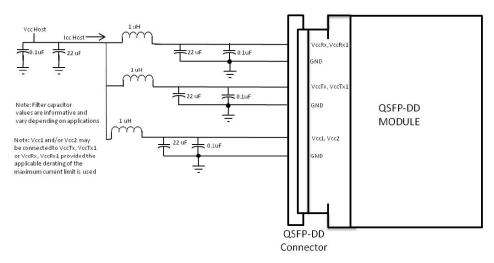


Figure 3. Host Board Power Supply Filtering





Optical Interface Lanes and Assignment

The optical interface port is a male MPO24 connector.

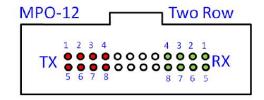


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP DD products. A 2-wire serial interfaceprovides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

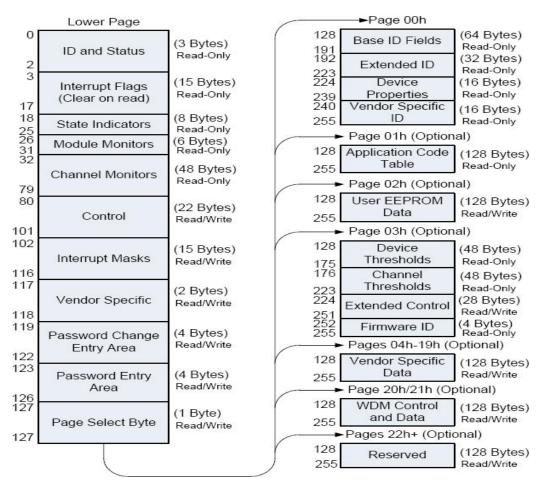


Figure 5. QSFP28 Memory Map

Table 16- Lower Page Overview (Lower Page)

Address	Description	Туре
0 - 2	Id and Status (3 bytes)	Read-only
3 - 17	Interrupt Flags (15 bytes)	Read-only
18 - 25	State Indicators (8 bytes)	Read-only
26 - 31	Module card Monitors (6 bytes)	Read-only
32 - 79	Channel Monitors (48 bytes)	Read-only
80 - 101	Control Fields (22 bytes)	Read/Write
102 - 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 - 118	Reserved	Read/Write
119 - 122	Password Change Area (4 bytes)	Write-Only
123 - 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map





Table 28- Upper Page 0 Overview (Page 00h)

		Table 20- opper	rage o everylen (rage con)
Address	Size (bytes)	Name	Description
Base ID H	rields:	1	
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper	Nominal laser wavelength

		cable Attenuation	(wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended	ID Field	S:	
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Sp	ecific I	D Fields:	
240-255	16	Vendor-Specific	Vendor-specific ID information
	20	NA CONTRACTOR OF THE PARTY OF T	Vo.

Figure 7. Page 00 Memory Map





Timing for Soft Control and Status Functions

Table 13	Timing for	OSFP-DD s	oft control	and status	functions
Table 13-	i imina toi	USFP-DD S	SOTE CONTROL	and status	runctions

	AND AND THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY.				
Parameter	Symbol	Min	Max	Unit	100
	Max MgmtInit		2000	ms	Time from power on2, hot plug or
MgmtInitDuration	Duration				rising edge of reset until completion
		9	80	18 3	of the MgmtInit State
ResetL Assert Time	t reset init	2		μs	Minimum pulse time on the ResetL
			10	188	signal to initiate a module reset.
IntL Assert Time	ton IntL		200	ms	Time from occurrence of condition
		4.	00		triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff IntL		500	μs	Time from clear on read ³ operation of
	_				associated flag until Vout:IntL=Voh.
					This includes deassert times for Rx
					LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS state to Rx LOS bit
	33.		8		set (value = 1b) and IntL asserted.
Rx LOS Assert Time	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit
(optional fast mode)	- 3		10		set (value = 1b) and IntL asserted.
Rx LOS Deassert Time	toff_losf		3	ms	Time from signal present to negation
(optional fast mode)		The state of the s			of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault
					bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition
					triggering flag to associated flag
	47	de:	er,	4	bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) 1
					until associated IntL assertion is
	ř.		0		inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared
	V.5000				(value=0b)1 until associated IntL
	8		8		operation resumes
Application or Rate	t_ratesel		100	ms	Time from change of state of
Select Change Time	90.5%				Application or Rate Select bit until
					transmitter or receiver bandwidth is
					in conformance with appropriate
			55		specification
					e stop bit of the write transaction
				then su	upply voltages reach and remain at or
above the minimum lev					
Note 3. Measured fro	om the rising e	edge o	f SDA	in the	stop bit of the read transaction

Figure8. Timing Specifications

Mechanical Dimensions

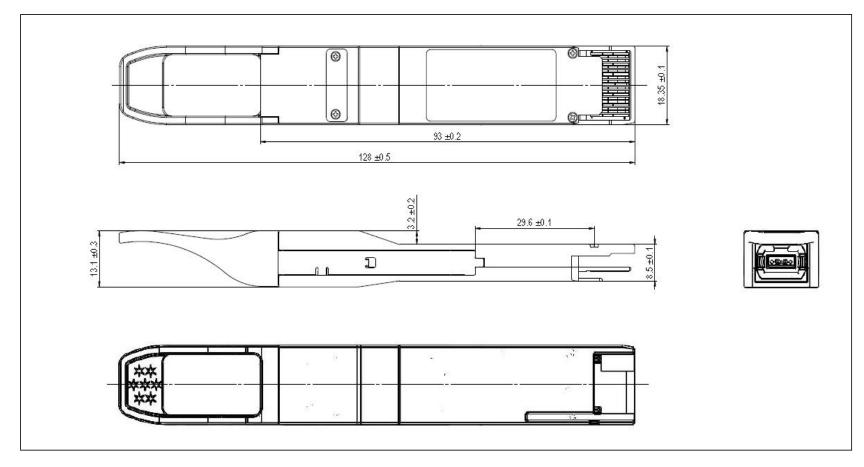


Figure 9. Mechanical Specifications





Regulatory Compliance

FIBERSTAMP FEL-200P8K02C are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard	
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	
		IEC 60825-1:2014	
Laser Eye Safety	TÜ∨	EN 60825-1:2014	
		EN 60825-2:2004+A1+A2	
Electrical Safety	TÜ∨	EN 60950-1:2006+A11+A1+A12+A2	
Electrical Safety	UL/CSA	UL 60950-1 & CAN/CSA C22.2 No.60950-1	
		CLASS 3862.07	
		CLASS 3862.87	
EMC	FCC	47 CFR FCC Part 15 Subpart B	
EMC	CE-EMC	EN 55032:2015	
		EN 55024:2010+A1:2015	
		EN 61000-3-2:2014	
		EN 61000-3-3:2013	

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

References

QSFP DD MAS Rev4.0

Ethernet 100GBASE-PSM4 IEEE802.3bm



Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description	
FEL-200P8K02C	QSFP DD, 2x100GBASE-PSM4, MPO Connector, reach 2km on G.652	

Important Notice

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