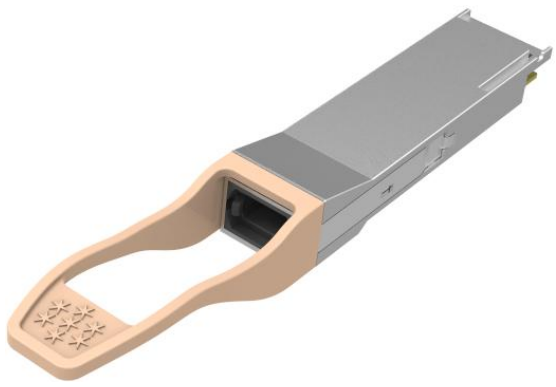
200G QSFP56 VR2 (4x53G PAM4 to 2x106G PAM4) 50m

Optical Transceiver Module

P/N: FEH-200S2M03C

Features

- ✓ 4x53.125Gbit/s PAM4 electrical interface(200GAUI-4)
- ✓ 2x106.25Gbps(53.125GBd PAM4) Optics architecture
- ✓ 2 channels 850nm VCSEL
- ✓ 2 channels PIN photo detector
- ✓ Power consumption <5W
- ✓ Hot Pluggable QSFP56 form factor and Compliant with CMIS V4.0
- ✓ Maximum link length of 30m on OM3 Multimode Fiber (MMF)and 50m on OM4 MMF with FEC
- ✓ MPO12 APC connector receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 10°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)



Applications

- ✓ IEEE 802.3db 400GBASE-SR4 Ethernet (PAM4)
- ✓ The transceiver is designed for Ethernet, Telecom and Infiniband use cases.

Description

The FIBERSTAMP FEH-200S2M03C is a Pluggable, Parallel, Fiber-Optic QSFP56 for 200 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnection applications. This module can convert 4-channel 53.125 Gbit/s electrical data to 2 parallel channels of optical signals, each supporting106.25 Gbit/s data transmission. Reversely, it can convert 2-channel 106.25 Gbit/s optical signals to 4-channel electrical output data on the receiver side. Each lane can operate up to 30 m using OM3 fiber or 50 m using OM4 fiber with FEC. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The optical interface uses 12 fiber MTP (MPO) connector. The Common Management Interface Specification (CMIS) for QSFP56 modules, This module incorporates FIBERSTAMP Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

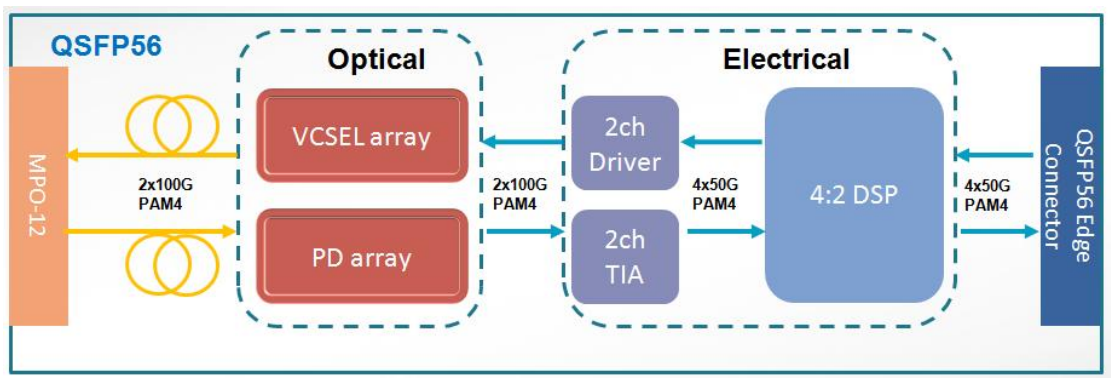


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating	Top	10	70	°C
Humidity(non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	10		70	°C
Data Rate Per Lane(line side)			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		4.5	5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage	ΔVin	400		900	mVp-p
Differential output voltage	ΔVout			850	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V
Input Logic Level High	V_{IH}	2.0		V_{cc}	V

Note：

1. BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	844	850	948	nm	_
RMS spectral width	Δλ	-	-	0.6	nm	_
Average launch power, each lane	Pout	-4.6	-	5	dBm	-
Optical Modulation Amplitude (OMAouter), each lane	OMA	-2.6		4	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ),each	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Receiver						
Centre Wavelength	λc	842	850	948	nm	-
Receiver Sensitivity in OMAout	RXsen			max (-4.4,TECQ 6.2)	dBm	1
Stressed Receiver Sensitivity in OMAout	SRS			-2	dBm	2
Maximum Average power at receiver , each lane				5	dBm	-

Minimum Average power at receiver , each		-6.4			dBm	
Receiver Reflectance				-15	dB	-
LOS Assert	LOSA	-15		-8.5	dBm	-
LOS De-Assert	LOSD			-6.5	dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[Note1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground [Note1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[Note1]
8	LVTTL-I	MODSEIL	Module Select[Note2]
9	LVTTL-I	ResetL	Module Reset[Note2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[Note2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[Note2]
13		GND	Module Ground[Note1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[Note1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[Note1]
20		GND	Module Ground[Note1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[Note1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[Note1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[Note2]
32		GND	Module Ground[Note1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[Note1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[Note1]

Note:

Note1. Module circuit ground is isolated from module chassis ground within the module.

Note2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

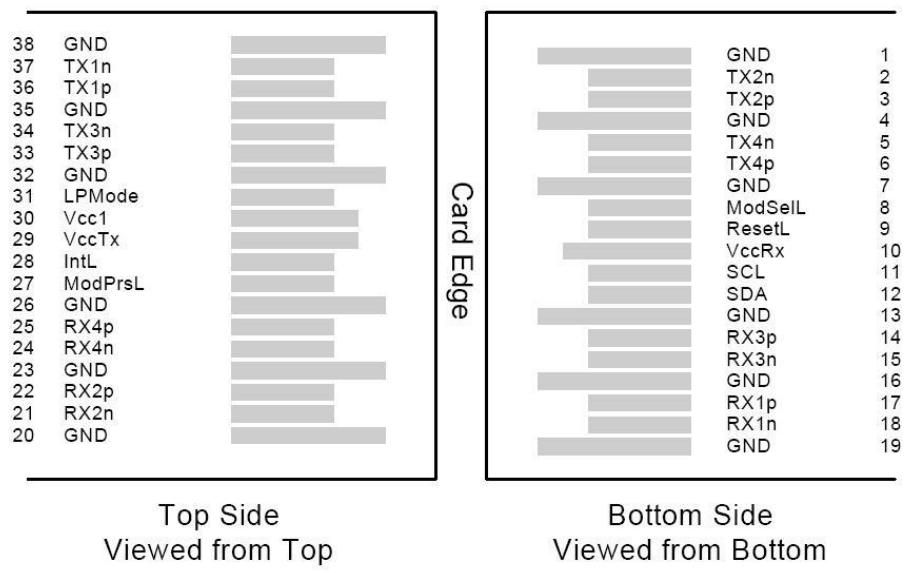


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

FIBERSTAMP QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

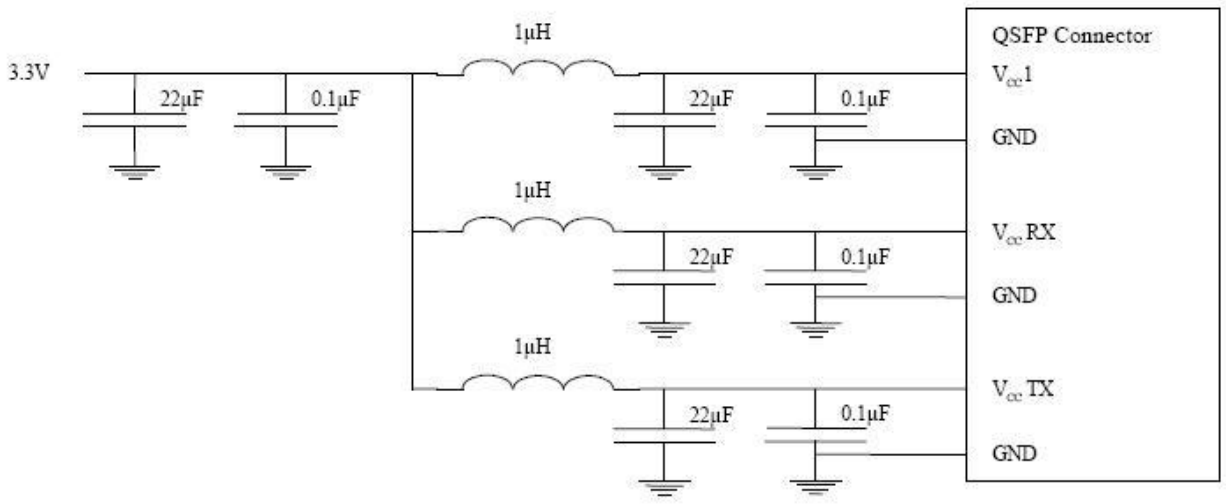


Figure3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 4.

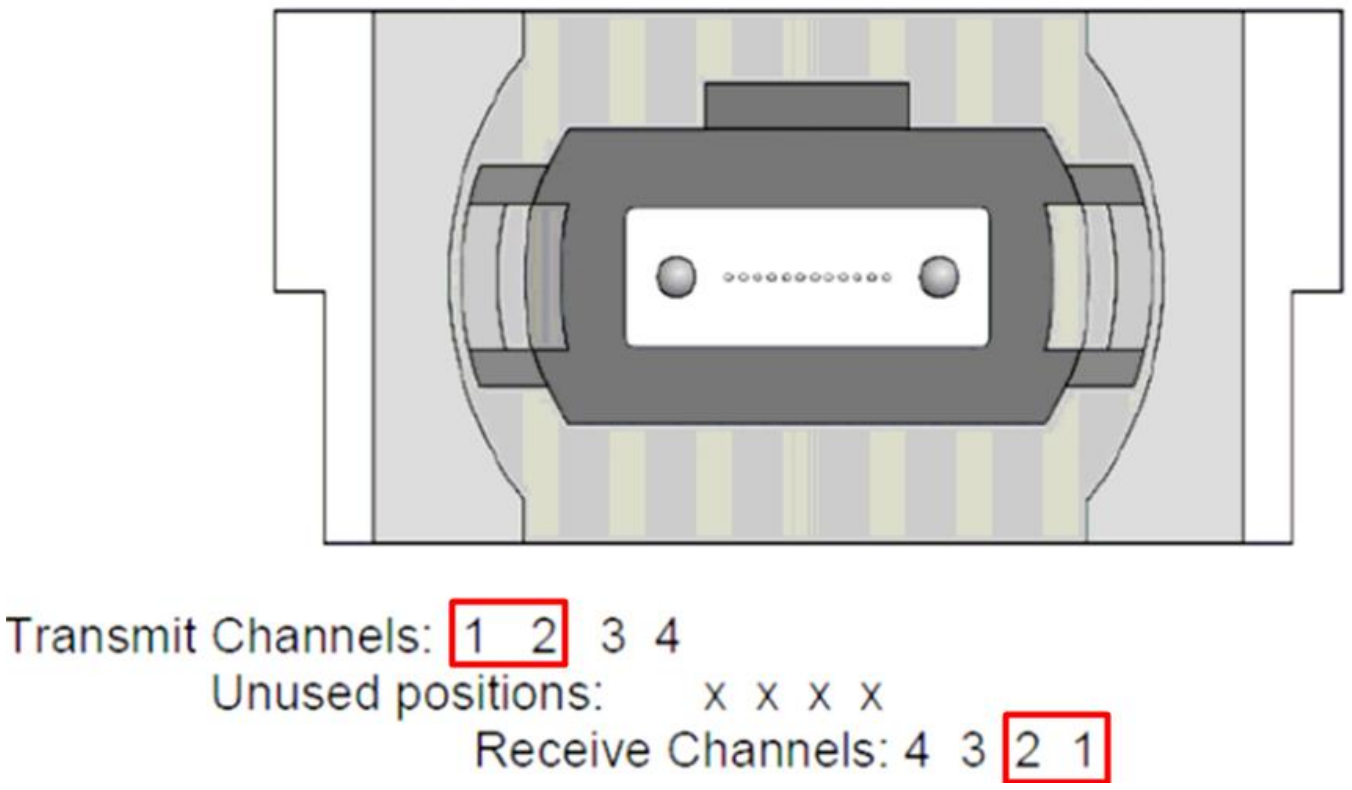


Figure 4. Optical Receptacle and Channel Orientation(Use the channel 1 and 2)

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP56 products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host

addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

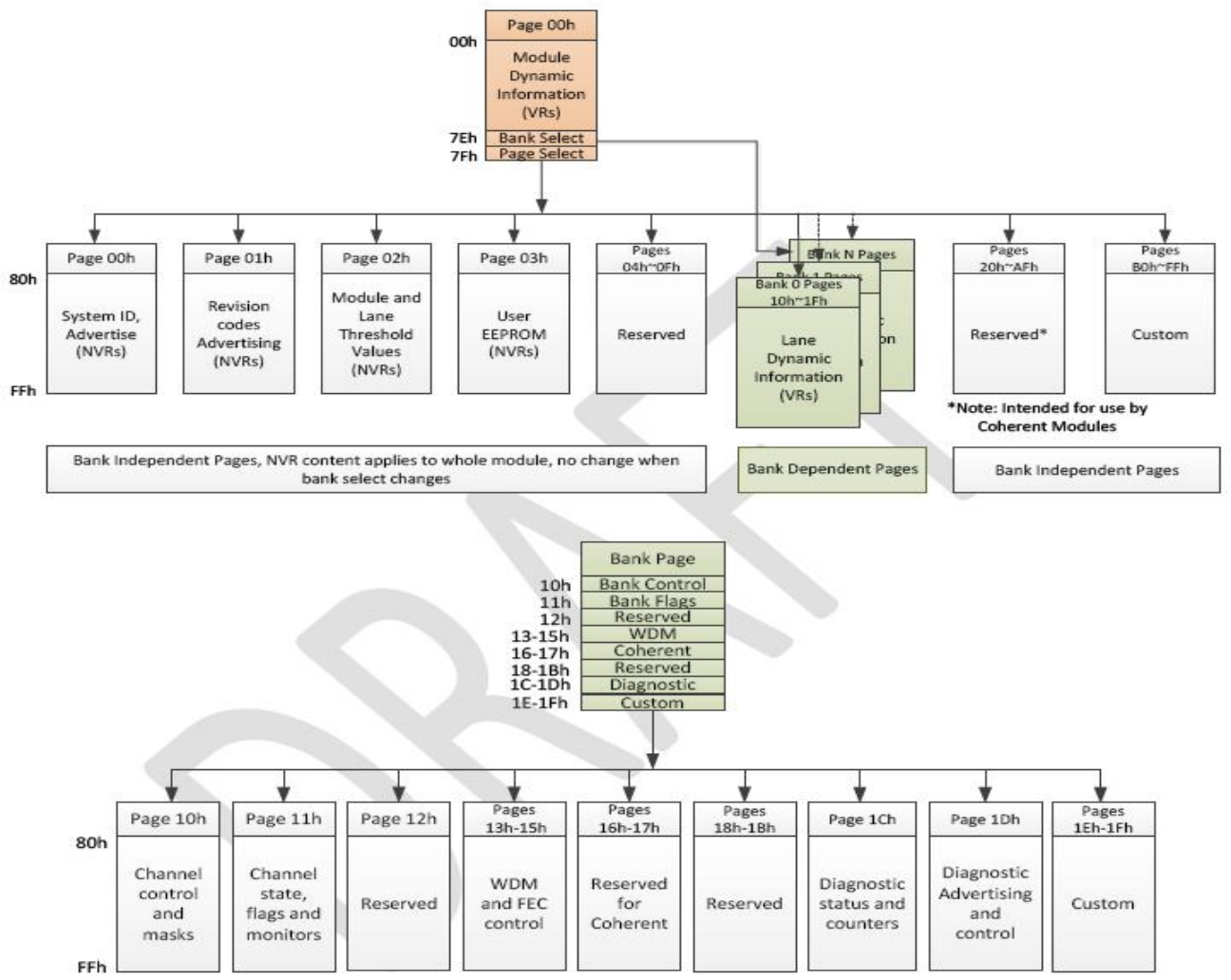


Figure5. QSFP56 Memory Map

Mechanical Dimensions(mm)

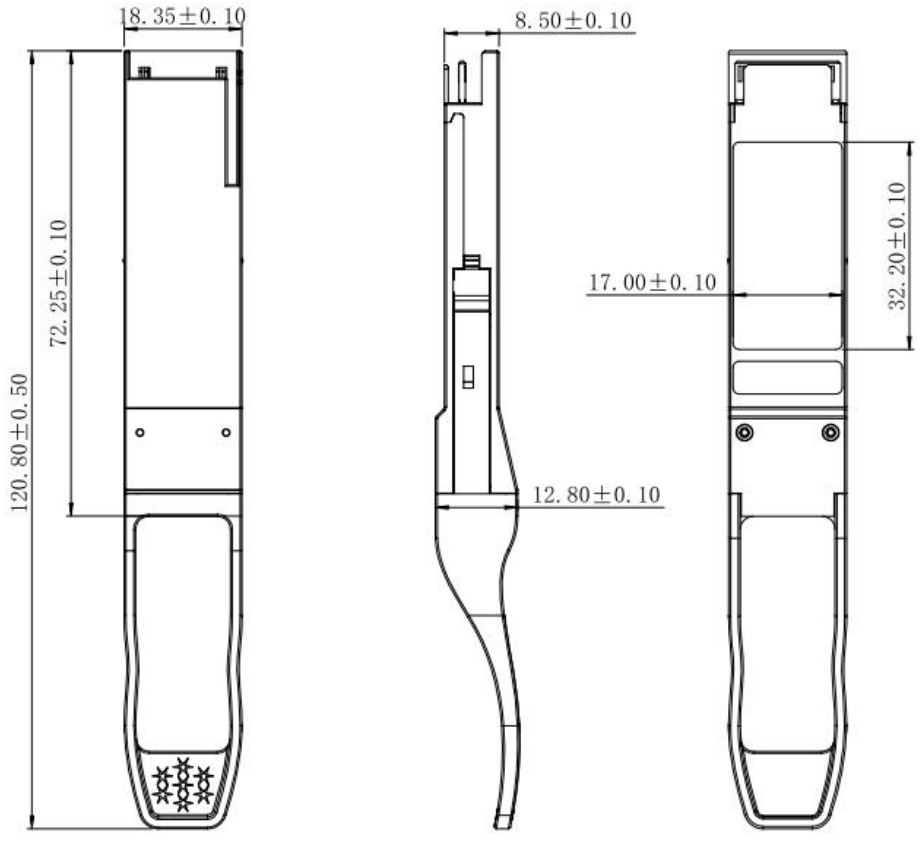


Figure6. Mechanical Specifications

Regulatory Compliance

Gigaligth FEH-200S2M03C transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP MSA
2. CMIS V4.0
3. IEEE 802.3db400GBASE-SR4 Ethernet (PAM4)

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FEH-200S2M03C	200G QSFP56 VR2(4x53G PAM4 to 2x106G PAM4) transceiver, MPO-12 APC interface, 850nm, up to 50m with OM4

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Revision History

Revision	Date	Description
V0	May-16-2025	Advance Release.