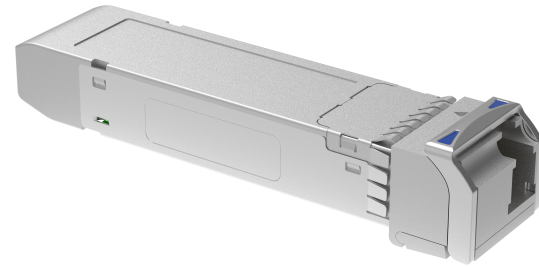


# 12Gbps Video SFP Optical Receiver, 20km Reach

## FFB-V12K20CM

### Features

- SD/HD/3G/6G/12G-SDI SFP Receiver
- ST 259, ST 292-1, ST 424, ST-2081 and ST-2082 compatible
- Metal enclosure for Lower EMI
- Supports video pathological patterns for SD-SDI, HD-SDI, 3G-SDI, 6G-SDI and 12G SDI
- With reclocker in the module
- Compliant with SFP MSA
- ROHS compliant (lead free)
- single 3.3V power supply
- Hot-pluggable SFP footprint
- Operating case temperature range: 0 to +70°C



### Applications

- Serial Digital Fiber Transmission System for SMPTE ST 259, SMPTE ST 344, SMPTE ST 292-1/2, SMPTE ST 424, SMPTE ST 2081-1 and SMPTE ST 2082-1 Signals
- UHDTV/HDTV/SDTV Service Interfaces

### Description

FIBERSTAMP's Video Receiver is designed to receive data rates from 50Mbps to 11.88Gbps, compliant with SMPTE ST 2082-1 (12G UHD-SDI), ST 2081-1 (6G UHD-SDI), ST424 (3G SDI), ST 292-1 (HD-SDI), and ST 259 (SD-SDI). FIBERSTAMP's Video Receiver supports SDI pathological patterns signals.

The Receiver includes these sections: a PIN photodiode integrated with a trans-impedance preamplifier (TIA), Reclocker, and a MCU controller. They are Compliant with SFP MSA

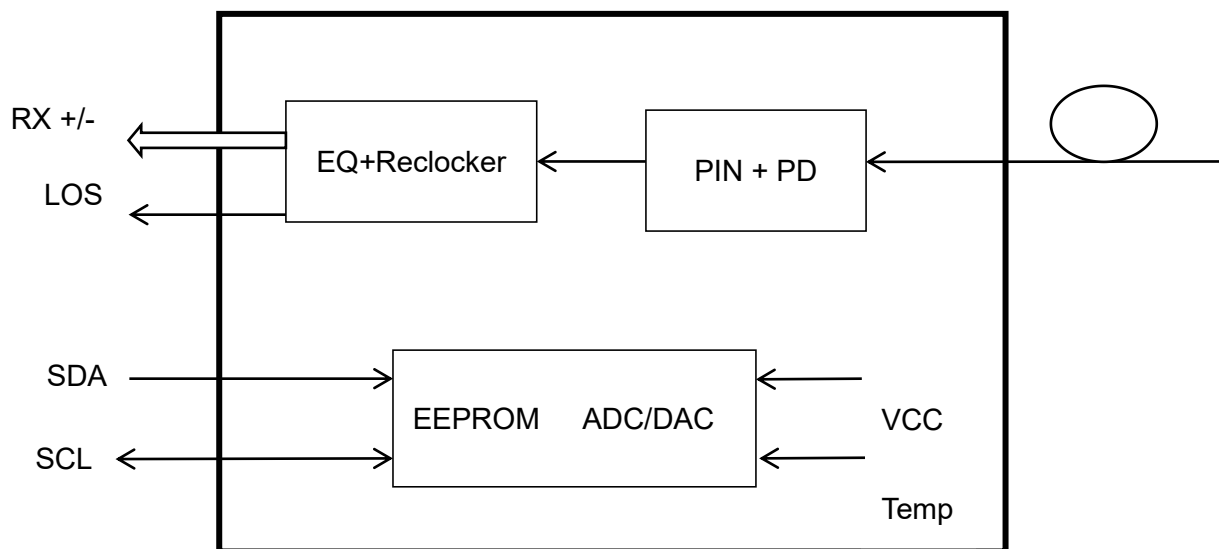


Figure 1. Module Block Diagram



### Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.5	5.25	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	-	5	85	%

### Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc		150		mA
Data Rate			12		Gbps

### Optical and Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	$\lambda_c$	1260		1580	nm	
Receiver Sensitivity@ 11.88Gbps				-11	dBm	1
Receiver Sensitivity@ 5.94Gbps				-13	dBm	
Receiver Sensitivity@ 2.97Gbps				-15	dBm	
Receiver Overload		1			dBm	2
LOS De-Assert	LOSD			-18	dBm	
LOS Assert	LOSA	-28			dBm	
LOS Hysteresis	LOSH	1		4	dB	
Data Output Swing Differential	Vout	400	800	800	mV	3
LOS	High	2.0		Vcc	V	
	Low			0.8	V	

#### Note:

1. Measured With Pathological Patterns 11.88Gbps (4096\*2160 P60,100% Bars);5.94Gbps (4096\*2160 P29.97,100% Bars);2.97Gbps (2048\*1080 P50,100% Bars).
2. Internally AC-coupled, minimum input overload power for SMPTE ST 2081-1, SMPTE ST 2082-1.
3. Rise and fall times, 20% to 80%.

### Timing and Electrical

Parameter	Symbol	Min	Typical	Max	Unit
Time To Initialize	t_init			300	ms
Serial ID Clock Rate	f_serial_clock		100		KHz
MOD_DEF (0:2)-High	VH	2		Vcc	V
MOD_DEF (0:2)-Low	VL			0.8	V

### Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
temperature	0 to +70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
RX Power	-24to +1	dBm	±3dB	Internal / External

### I<sup>2</sup>C Bus Interface

The I<sup>2</sup>C bus interface uses the 2-wire serial CMOS E2PROM protocol. The serial interface meets the following specifications:

1. Support a maximum clock rate of 280Khz.
2. Input/Output levels comply with LVCMOS/LVTTL or compatible logics.

Low: 0 - 0.8 V

High: 2.0 - 3.3 V

Undefined: 0.8 - 2.0 V

### Pin Description

Pin	Signal Name	Description	Plug Seq.	Notes
1	VEE	Ground	1	
2	VEE	Ground	3	
3	NC	Not Connected	3	
4	MOD_DEF(2)-SDA	2-wire Serial Interface Data Line	3	Note 1
5	MOD_DEF(1)-SCL	2-wire Serial Interface Clock	3	Note 1
6	MOD_DEF(0)-PRESENCE (VEE)	TTL Low	3	Note 1
7	Rate (NC)	Not Connected	3	
8	LOS	Loss of Signal	3	Note 2
9	VEE	Ground	3	
10	VEE	Ground	1	
11	VEE	Ground	1	
12	RX-	Receiver Inverted Data Output	3	Note 3
13	RX+	Receiver Non-Inverted Data Output	3	Note 3
14	VEE	Ground	1	
15	VCC	Receiver Power Supply	2	
16	VCC	Receiver Power Supply	2	
17	VEE	Ground	1	
18	NC	Not Connected	3	
19	NC	Not Connected	3	
20	VEE	Ground	1	

#### Note:

Plug Seq.: Pin engagement sequence during hot plugging.

1. Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7k~10kΩ resistor on the host board.

The pull-up voltage shall be  $V_{ccT}$  or  $V_{ccR}$ .

Mod-Def 0 is grounded by the module to indicate that the module is present.

Mod-Def 1 is the clock line of two wire serial interface for serial ID.

Mod-Def 2 is the data line of two wire serial interface for serial ID.

- LOS is an open collector output, which should be pulled up with a  $4.7k\sim 10k\Omega$  resistor on the host. Pull up voltage between 2.0V and  $V_{cc}+0.3V$ . Logic 1 indicates loss of signal; Logic 0 indicates normal operation. In the low state, the output will be pulled to less than 0.8V.
- RX-/+ : These are the differential receiver outputs. They are internally AC-coupled 100 differential lines which should be terminated with  $100\Omega$  (differential) on the host.

## Pin Definition

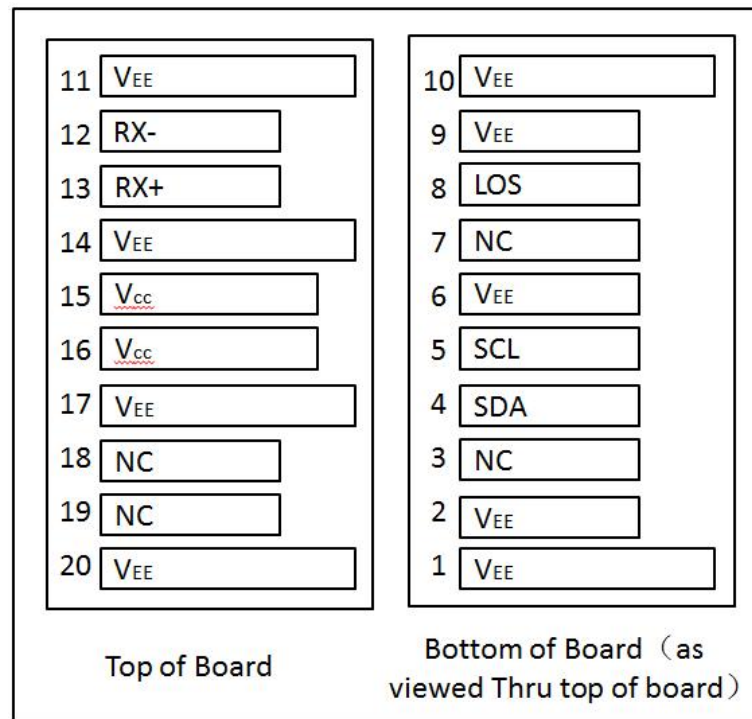


Figure 2. Electrical Pin-out Details

## Mechanical Dimensions

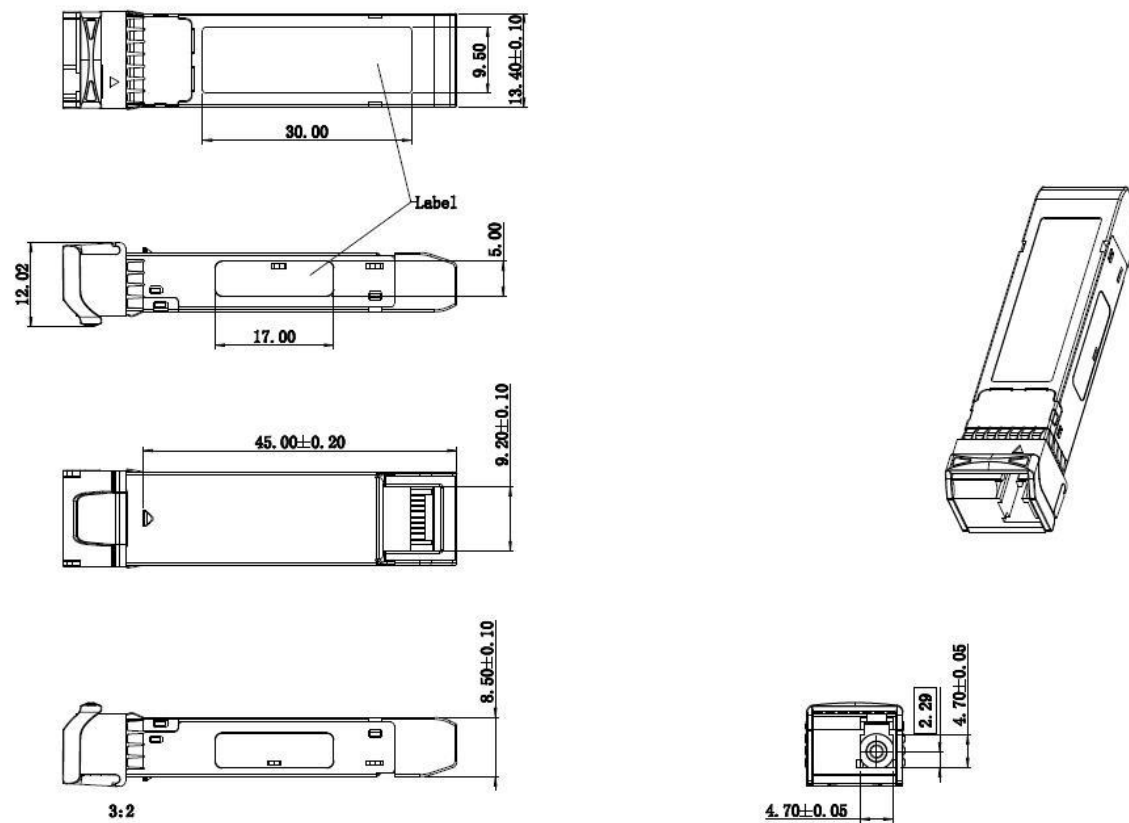


Figure 3. Mechanical Specifications

**Regulatory Compliance**

Feature	Standard
Environmental protection	2011/65/EU
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014
Product Safety	EN/UL 60950-1, 2nd Edition, 2014-10-14

**⚠️ CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

**Ordering Information**

Part Number	Product Description
FFB-V12K20CM	SD/HD/3G/6G/12G SDI Receiver, MSA , Reclocker

**Important Notice**

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