

100G CFP to QSFP28 Adapter

Features

- Hot-pluggable CFP form factor
- Convert 10 bidirectional 10G lanes to 4 bidirectional 25G lanes
- 1 port QSFP28 TX&RX (FEC configurable)
- Supports 100G IEEE 802.3bj NRZ FEC
- Compliant with CFP MSA, CMIS, 100GE and OTN OTU4
- Data rate up to 111.8Gbps
- Power consumption < 5W
- MDIO management interface
- Operating case temperature range from 0°C to 70°C
- 3.3V power supply voltage
- RoHS compliant (lead free)



Applications

- 100GBE interconnects, IEEE 802.3ba 100GBASE-LR4(Adapter+QSFP28_LR4), IEEE 802.3bm 100GBASE-SR4(Adapter+QSFP28_SR4)
- High-speed core router connections& Datacom/Telecom switch
- Data aggregation and backplane applications
- Proprietary protocol and density application

Description

The 100G CFP to QSFP28 Adapter module is a high performance, hot pluggable, and interconnect solution supporting 100G Ethernet and Telecom. The Adapter converts a CFP MSA interface to 1-port of 100GE QSFP28. It is compliant with the CFP MSA. FiberStamp 100G CFP to QSFP28 Adapter module converts 10 bidirectional 10G channels to 4 bidirectional 25G channels operating at up to 28Gbps per channel. The Adapter supports FEC (Forward Error Correction) function; the user can enable the FEC function through the register configuration.

As shown in Figure 1, the transmitter side of the adapter converts 10 parallel electrical data inputs to 4 parallel electrical data output signals through a 10:4 multiplexing and associated circuitry. The receiver side of the adapter converts 4 parallel electrical signals into 10 parallel electrical signals through a 4:10 De multiplexing and associated circuitry.

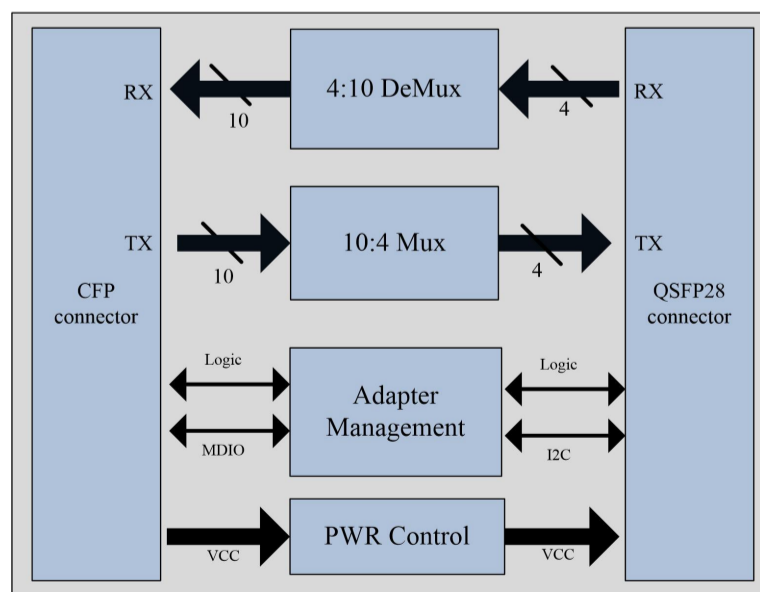


Figure1. Adapter Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.5	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Humidity(non-condensing)	Rh	5	85	%

*Exceeding any one of these values may destroy the device immediately

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Operating Case temperature	Tca	0		70	°C	
Data RatePer Lane	10GBE	fd	-	10.3125	11.2	Gbps
	25GBE			25.78125	27.952	
Power Dissipation	Pm			5	W	
Low Power Mode Dissipation	Plow			2	W	
Aggregate Bit Rate	BRaggr		103.125	111.8	Gbps	

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
10GBE	Differential input voltage amplitude	ΔV_{in}	120	820	mVp-p	1
	Differential output voltage amplitude	ΔV_{out}	300	820	mVp-p	2
25GBE	Differential input voltage amplitude	ΔV_{in}	300	1100	mVp-p	1
	Differential output voltage amplitude	ΔV_{out}	500	900	mVp-p	2
Bit Error Rate	BER			E-12		3
Input Logic Level High	VIH	2.0		VCC+0.3	V	3.3V LVCOMS
		0.84		1.5	V	1.2V LVCOMS
Input Logic Level Low	VIL	-0.3		0.8	V	3.3V LVCOMS
		-0.3		0.36	V	1.2V LVCOMS
Output Logic Level High	VOH	VCC-0.2		VCC	V	3.3V LVCOMS
		1.0		1.5	V	1.2V LVCOMS
Output Logic Level Low	VOL	0		0.2	V	3.3V LVCOMS
		-0.3		0.2	V	1.2V LVCOMS



Notes:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.
3. BER=10⁻¹²; PRBS 2³¹-1@10.3125Gbps/25.78125Gbps.

Reference Clock Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125 / 644.53125	174.7030837 / 698.8123348	MHz	1/64 or 1/16 of electrical lane rate
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
RMS jitter	σ			10	ps	Random Jitter. Over frequency band of 10KHz < f < 10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	tr/f	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

FEC control register

Address	AccessType	BitWidth	Description	Notes
0x91FC	R/W	1	0x0: Enable FEC. 0x1: Disable FEC.	FEC is invalid when OTU4 data rate mode is on

FEC control register 0x91FC supports reconfiguration and save function:

1. Write value to 0x91FC;
2. Read the address 0xA004 = 0000h (Idle);
3. Save command, writes value 0001h to address 0x91F0;
4. Read status, wait until the address 0xA004 = 0004h (save success), and then read the address again 0xA004 = 0000h (Idle, read twice to ensure status is cleared).
5. Normally saving needs about 1 second, but the longest time is about 4 seconds, we suggest customer can read 0xA004 after waiting for a while.

Register Map

100G CFP to QSFP28 Adapter is compliant to CFP MSA Management Interface Specification Version 2.2. The addresses correspond to CFP MSA Management Interface Specification V2p2rev06a. Not all the QSFP28 I2C registers are remapped. Some registers are illustrated in Table 1. Other registers also correspond to CFP MSA MDIO MIS (Management Interface Specification V2p2rev06a). The QSFP28 I2C registers (DDM Monitor and Alarm/Warning register) are remapped into the CFP MDIO register map. The Adapter can provide CFP Module State transition, FAWS signal, Bit Error Rate Calculation, User NVR Restore and Save Functions and DDM monitor. It makes the optic look exactly like a CFP module.



Table1: Some of the 100G CFP to QSFP28 Adapter register

CFP NVR 1 Table. Basic ID registers.			
HexAddr	Register Name	Description	Note
8000	Module Identifier	Default value is 0Eh: CFP	1
8001	Extended Identifier	Default value is 50h: Power Class 2, Gear Box type	1
8002	Connector Type Code	The value corresponds to QSFP28 I2C register(Address A0h, byte 130(Page 00))	1,2
8003	Ethernet Application Code	Default value is 01h: 100GE-LR4	1
8004~8007	Application Code	Default value is 00h:Undefined type	1
8008	Additional Capable Rates Supported	Default value is 18h:Support 111.8 Gbps and 103.125 Gbps	1
8009	Number of Lanes Supported	Default value is 4Ah: 4 Network Lanes and 10 Host Lanes	1
800A	Media Properties	Default value is 84h	1
800B	Maximum Network Lane Bit Rate	Default value is 8Ch: 28Gbps	1
800C	Maximum Host Lane Bit Rate	Default value is 38h: 11.2Gbps	1
800D	Maximum Single Mode Optical Fiber Length	Default value is 0Ah: 10km	1
800E	Maximum Multi-Mode Optical Fiber Length	Default value is 1Eh: 300m	1
800F	Maximum Copper Cable Length	Default value is 00h: undefined	1
8010	Number of Active Transmit Fibers	Default value is 04h	1
8011	Number of Wavelengths per active Transmit Fiber	Default value is 00h	1
8012~8015	Minimum and Wavelength per Active Fiber	The value corresponds to QSFP28 I2C register(Address A0h, byte 186~189(Page 00))	1,2
8016~8017	Maximum per Lane Optical Width	Default value is 00h	1
8018~8019	Device Technology	The value corresponds to QSFP28 I2C register(Address A0h, byte 147(Page 00))	1,2
801A	Signal Code	Default value is 40h	1
801B~801C	Maximum Total Optical Output Power per Connector and Maximum Optical Input Power per Network Lane	Default value is 00h: undefined	1
801D	Maximum Power Consumption	Default value is 00h: undefined	1
801E	Maximum Power Consumption in Low Power Mode	Default value is 64h: 2W	1
801F	Maximum Operating Case Temp Range	The value corresponds to QSFP28 I2C register(Address A0h, byte 190(Page 00))	1,2



CFP NVR 1 Table. Basic ID registers.			
HexAddr	Register Name	Description	Note
8020	Minimum Operating Case Temp Range	Default value is 00h	1
8021~805B	Vendor information	Reserved for Vendor	1
805C~8067	Lot Code and CLEI Code	Default value is 00h	1
8068	CFP MSA Hardware Specification Revision Number	Default value is 0Eh: V1.4	1
8069	CFP MSA Management Interface Specification Revision Number	Default value is 16h: V2.2	1
806A~806B	Module Hardware Version Number	Default V1.0	1
806C~806D	Module Firmware Version Number	Default V1.0	1
806E	Digital Diagnostic Monitoring Type	Default value is 0Ch: power measurement type(average Power)	1
806F	Digital Diagnostic Monitoring Capability 1	Default value is 03h	1
8070	Digital Diagnostic Monitoring Capability 2	Default value is 0Eh	1
8071	Module Enhanced Options	Default value is F8h	1
8072~8073	Maximum High-Power-up and TX-Turn-on Time	Default value is 01h	1
8074	Host Lane Signal Spec	Default value is 01h: CAUI	1
8075	Heat Sink Type	Default value is 00h	1
8076	Maximum TX-Turn-off Time	Default value is 0Ah	1
8077	Maximum High-Power-down Time	Default value is 01h	1
8078	Module Enhanced Options 2	Default value is 25h	1
8079~807A	Transmitter and Receiver Monitor Clock Options	Default value is 00h: not supported	1
807B~807C	Module Firmware B Version Number	Default value is 00h	1
807D	Maximum MDIO Ready Time	Default value is 03h	1
807E	CFP Extended Identifier	Default value is E0h	1
807F	CFP NVR 1 Checksum	The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.	
CFP NVR 2 Table: Alarm/Warning Threshold Registers			
HexAddr	Register Name	Description	Note



CFP NVR 1 Table. Basic ID registers.			
HexAddr	Register Name	Description	Note
8080~8087	Transceiver Temp Alarm/Warning Threshold	The value corresponds to QSFP28 I2C Temp register(Address A0h, byte 128~135(Page 03))	1,2
8088~808F	VCC Alarm/Warning Threshold	The value corresponds to QSFP28 I2C VCC threshold register(Address A0h, byte 144~151 (Page 03))	1,2
8090~80A7	Alarm/Warning Threshold	Reserved or undefined	1
80A8~80AF	Laser Bias Current Alarm/Warning Threshold	The value corresponds to QSFP28 I2C Tx Bias threshold register(Address A0h, byte 184~191 (Page 03))	1,2
80B0~80B7	Laser Output Power Alarm/Warning Threshold	The value corresponds to QSFP28 I2C TX Power threshold register(Address A0h, byte 192~199 (Page 03))	1,2
80C0~80C7	Receive Optical Power Alarm/Warning Threshold	The value corresponds to QSFP28 I2C RX Power threshold register(Address A0h, byte 176~183 (Page 03))	1,2
80C8~80FE	Alarm/Warning Threshold	Reserved or undefined	1
80FF	CFP NVR 2 Checksum	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.	
CFP Module VR 1. CFP Module level control and DDM registers.			
HexAddr	Register Name	Description	Note
A01F	Module Alarms and Warnings 1	The value corresponds to QSFP28 I2C Alarms and Warning register(Address A0h, byte 6~7)	3
A02F	Module Temp Monitor A/D Value	The value corresponds to QSFP28 I2C Temp Monitor register(Address A0h, byte 22~23)	3
A030	Module Power supply 3.3 V Monitor A/D Value	The value corresponds to QSFP28 I2C Supply Voltage register(Address A0h, byte 26~27)	3
Network Lane VR : Network Lane Specific Register and A/D value Measurement Registers			
HexAddr	Register Name	Description	Note
A200~A203	Network Lane n Alarm and Warning	The value corresponds to QSFP28 I2C Channel Monitor Interrupt Flags register(Address A0h, byte 9~14)	3
A210~A213	Network Lane n Fault and Status	The bit[4] and bit[7] values correspond to QSFP28 I2C Channel Status Interrupt Flags register(Address A0h, byte 3)	3
A2A0~A2A3	Network Lane n Laser Bias Current monitor A/D value	The value corresponds to QSFP28 Tx Bias monitor register(Address A0h, byte 42~49)	3
A2B0~A2B3	Network Lane n Laser Output Power monitor A/D value	The value corresponds to QSFP28 TxPower monitor register(Address A0h, byte 50~57)	3
A2D0~A2D3	Network Lane n Receiver Input Power monitor A/D value	The value corresponds to QSFP28 I2C RxPower monitor register(Address A0h, byte 34~41)	3



Notes:

1. CFP NVR 1 and CFP NVR 2 Tables have initial values. If customer need access to CFP NVR 1 and CFP NVR 2 Table, we can OPEN write access.
2. When QSFP28 module present, firstly, read values from QSFP28 I2C registers and maps into the CFP MDIO registers.
3. When QSFP28 module present, the alarm/warning data and DDM data update periodically during the whole operation of the module, the maximum data refresh period is 200ms.

CFP Connector Pin Descriptions

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description
1	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND	GND		
3	3.3V_GND	GND		
4	3.3V_GND	GND		
5	3.3V_GND	GND		
6	3.3V	VCC		3.3V Module Supply
7	3.3V	VCC		
8	3.3V	VCC		
9	3.3V	VCC		
10	3.3V	VCC		
11	3.3V	VCC		
12	3.3V	VCC		
13	3.3V	VCC		
14	3.3V	VCC		
15	3.3V	VCC		
16	3.3V_GND	GND		
17	3.3V_GND	GND		
18	3.3V_GND	GND		
19	3.3V_GND	GND		
20	3.3V_GND	GND		
21	NC		I/O	FiberStamp internal, do not connect
22	NC		I/O	FiberStamp internal, do not connect
23	GND	GND		
24	(TX_MCLKn)	CML	O	CML For optical waveform testing. Not used.
25	(TX_MCLKp)	CML	O	CML For optical waveform testing. Not used.
26	GND	GND		
27	NC		I/O	FiberStamp internal, do not connect
28	NC		I/O	FiberStamp internal, do not connect



Pin	Symbol	Type	I/O	Description
29	NC		I/O	FiberStamp internal, do not connect
30	PRG_CNTL1	LVC MOS w/PU	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn – TX & RX IC reset. "0" = reset, "1" or NC = enabled or not used
31	PRG_CNTL2	LVC MOS w/PU	I	Programmable Control 2 set via MDIO, MSA default: Hardware power Interlock LSB, "00" = <8W, "01" = <16W, "10" < 24W, "11" or NC = >24W or not used
32	PRG_CNTL3	LVC MOS w/PU	I	Programmable Control 3 set via MDIO, MSA default: Hardware power Interlock MSB, "00" = <8W, "01" = <16W, "10" < 24W, "11" or NC = >24W or not used
33	PRG_ALARM1	LVC MOS	O	Programmable Alarm 1 set via MDIO, Reflex default: HIPWR_ON, Module power on indicator. "1" = Module high power up completed, "0" = Module not high powered up
34	PRG_ALARM2	LVC MOS	O	Programmable Alarm 2 set via MDIO, Reflex default: MOD_READY, module initialization complete, "1" = complete, "0" = not complete
35	PRG_ALARM3	LVC MOS	O	Programmable Alarm 3 set via MDIO, Reflex default: MOD_FAULT, module fault detected, "1" = fault, "0" = no fault
36	TX_DIS	LVC MOS w/PU	I	Transmitter Disable for all channels, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	LVC MOS w/PU	I	Module low power mode. "1" or NC = module in low power (safe) mode, "0" = power-on enabled
38	MOD_ABS	GND	O	Module Absent. "1" or NC = Module absent, "0" = module present. Pull-up resistor on Host
39	MOD_RSTn	LVC MOS w/PD	I	Module Reset. "0" = reset the module, "1" or NC = module enabled, Pull Down resistor in module
40	RX_LOS	LVC MOS	O	Receiver loss of optical signal on any channel, "1" = loss of signal, "0" = normal condition
41	GLB_ALRMn	LVC MOS	O	Global Alarm. "0" = alarm condition in any MDIO alarm register, "1" = no alarm
42	PRTADR4	1.2V CMOS	I	MDIO port address bit 4
43	PRTADR3	1.2V CMOS	I	MDIO port address bit 3
44	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
45	PRTADR1	1.2V CMOS	I	MDIO port address bit 1
46	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
47	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as per 802.3ae)
48	MDC	1.2V CMOS	I	Management data clock (electrical specs as per 802.3ae)
49	GND	GND		
50	NC		I/O	FiberStamp internal, do not connect
51	NC		I/O	FiberStamp internal, do not connect



Pin	Symbol	Type	I/O	Description
52	GND	GND		
53	NC		I/O	FiberStamp internal, do not connect
54	NC		I/O	FiberStamp internal, do not connect
55	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND	GND		
57	3.3V_GND	GND		
58	3.3V_GND	GND		
59	3.3V_GND	GND		
60	3.3V	VCC		3.3V Module Supply
61	3.3V	VCC		
62	3.3V	VCC		
63	3.3V	VCC		
64	3.3V	VCC		
65	3.3V	VCC		
66	3.3V	VCC		
67	3.3V	VCC		
68	3.3V	VCC		
69	3.3V	VCC		
70	3.3V_GND	GND		
71	3.3V_GND	GND		
72	3.3V_GND	GND		
73	3.3V_GND	GND		
74	3.3V_GND	GND		

Part B: Top Row Pin Function Definition

Pin	Symbol	Pin	Symbol
148	GND	111	GND
147	REFCLKn	110	Not used
146	REFCLKp	109	Not used
145	GND	108	GND
144	Not used	107	RX9n
143	Not used	106	RX9p
142	GND	105	GND
141	TX9n	104	RX8n
140	TX9p	103	RX8p
139	GND	102	GND



Pin	Symbol	Pin	Symbol
138	TX8n	101	RX7n
137	TX8p	100	RX7p
136	GND	99	GND
135	TX7n	98	RX6n
134	TX7p	97	RX6p
133	GND	96	GND
132	TX6n	95	RX5n
131	TX6p	94	RX5p
130	GND	93	GND
129	TX5n	92	RX4n
128	TX5p	91	RX4p
127	GND	90	GND
126	TX4n	89	RX3n
125	TX4p	88	RX3p
124	GND	87	GND
123	TX3n	86	RX2n
122	TX3p	85	RX2p
121	GND	84	GND
120	TX2n	83	RX1n
119	TX2p	82	RX1p
118	GND	81	GND
117	TX1n	80	RX0n
116	TX1p	79	RX0p
115	GND	78	GND
114	TX0n	77	Not used
113	TX0p	76	Not used
112	GND	75	GND

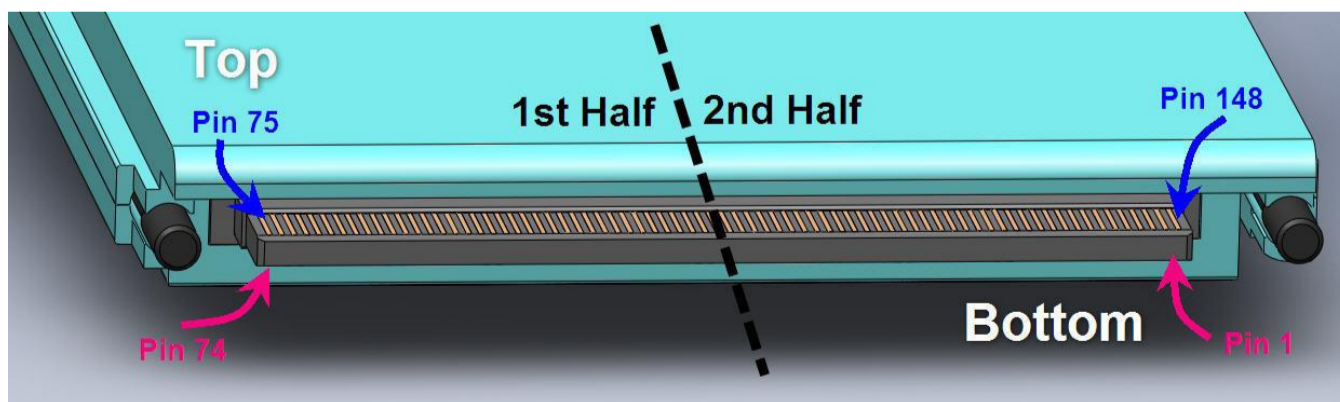


Figure2.Pad Layout of the CFP connector



QSFP28 Connector Pin Descriptions

Pin	Logic	Symbol	Description	
1		GND	Module Ground	1
2	CML-O	Tx2-	Transmitter inverted data output	
3	CML-O	Tx2+	Transmitter non-inverted data output	
4		GND	Module Ground	1
5	CML-O	Tx4-	Transmitter inverted data output	
6	CML-O	Tx4+	Transmitter non-inverted data output	
7		GND	Module Ground	1
8	LVTTTL-O	MODSEIL	Module Select	2
9	LVTTTL-O	ResetL	Module Reset	2
10		VCCR _x	+3.3v Receiver Power Supply	
11	LVC MOS-O	SCL	2-wire Serial interface clock	2
12	LVC MOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-I	RX3+	Receiver non-inverted data input	
15	CML-I	RX3-	Receiver inverted data input	
16		GND	Module Ground	1
17	CML-I	RX1+	Receiver non-inverted data input	
18	CML-I	RX1-	Receiver inverted data input	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-I	RX2-	Receiver inverted data input	
22	CML-I	RX2+	Receiver non-inverted data input	
23		GND	Module Ground	1
24	CML-I	RX4-	Receiver inverted data input	
25	CML-I	RX4+	Receiver non-inverted data input	
26		GND	Module Ground	1
27	LVTTTL-I	ModPrsL	Module Present, QSFP28 Module pulled down to GND	
28	LVTTTL-I	IntL	Interrupt input	2
29		VCCT _x	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTTL-O	LPM _{Mode}	Low Power Mode	2
32		GND	Module Ground	1
33	CML-O	Tx3+	Transmitter non-inverted data output	
34	CML-O	Tx3-	Transmitter inverted data output	
35		GND	Module Ground	1



Pin	Logic	Symbol	Description	
36	CML-O	Tx1+	Transmitter non-inverted data output	
37	CML-O	Tx1-	Transmitter inverted data output	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; pulled up with 4.7k ohms on the adapter board to a voltage 3.3V.

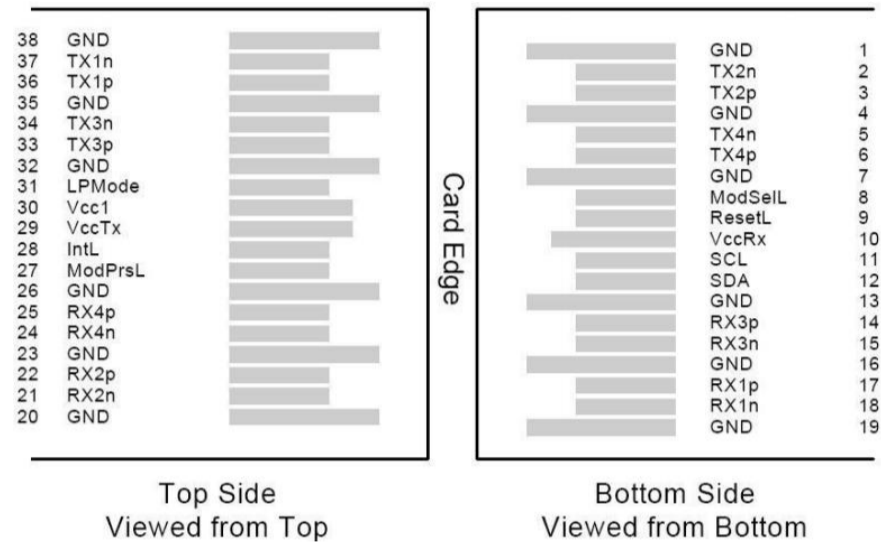
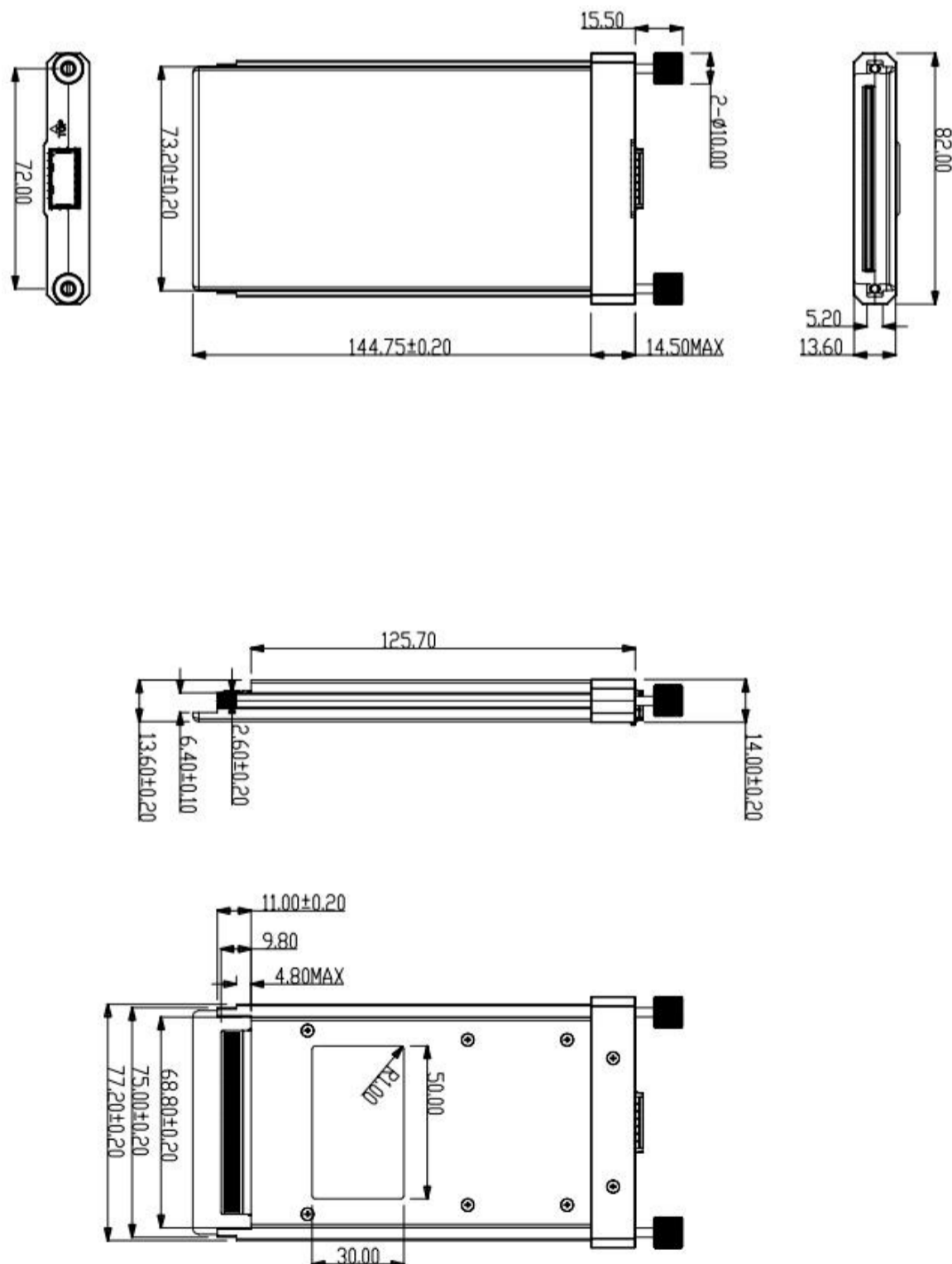


Figure3.Pad Layout of the QSFP28connector

Mechanical Dimensions



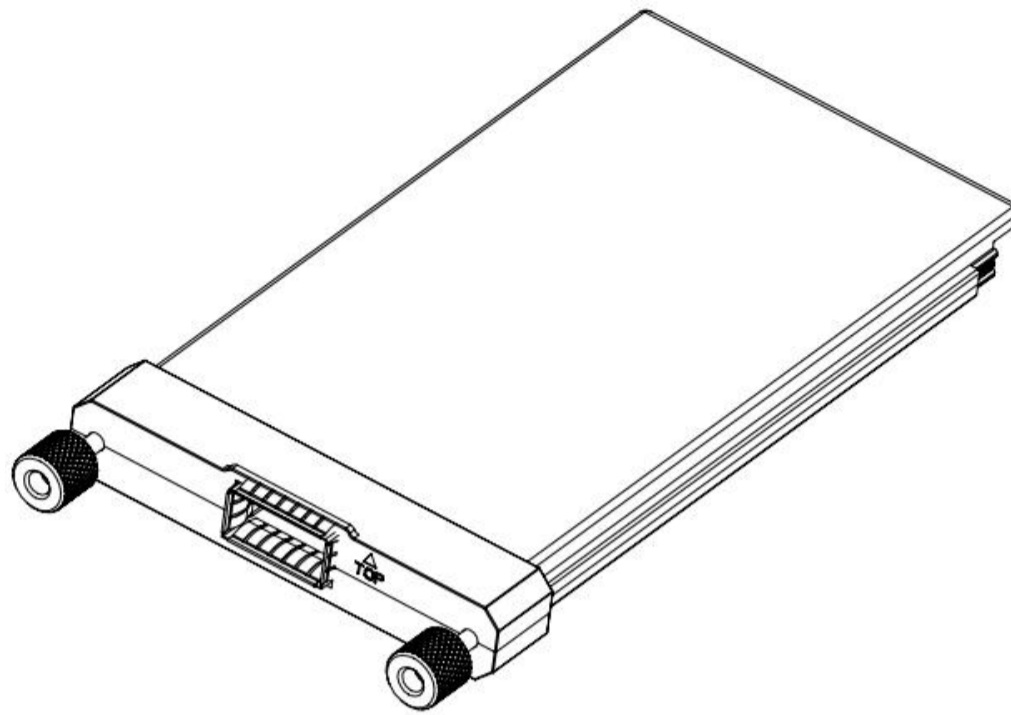


Figure 4. Mechanical Specifications

Ordering information

Part Number	Product Description
FSC-CFP-QSFP28	100G CFP to QSFP28 Adapter

Important Notice

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