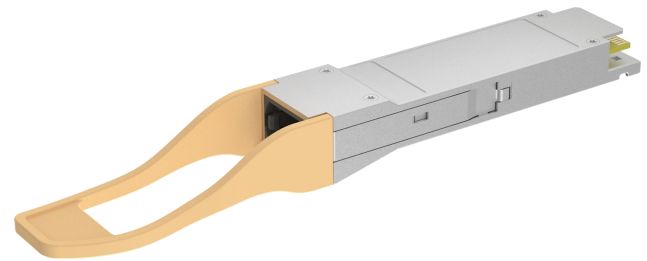


# 100GBASE-SR4 100m QSFP28 Optical Transceiver

## FEG-100S4M10C

### Features

- Hot-pluggable QSFP28 form factor
- 4 channels full-duplex transceiver module
- Supports 103.125Gb/s aggregate bit rate
- 4 channels 850nm VCSEL array
- 4 channels PIN photo-detector array
- Internal CDR circuits on both receiver and transmitter channels
- Supports CDR bypass
- 2W maximum power dissipation
- Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF
- Single MTP/MPO receptacle
- Operating case temperature range: 0 to 70°C
- Single 3.3V power supply
- RoHS compliant (lead free)



### Applications

100GBASE-SR4 100G Ethernet

### Description

The FIBERSTAMP 100GBASE-SR4 100m QSFP28 optical transceiver, 100G QSFP28 SR4 (FEG-100S4M10C) is designed for use in 100-Gigabit Ethernet links up to 100m over Multi-Mode Fiber (MMF). It is compliant with the QSFP28 MSA and IEEE 802.3bm 100GBASE-SR4 and CAUI-4. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA. It integrates 4 data lanes in each direction with 4x25.78125Gb/s bandwidth. The electrical interface uses a 38-contact edge type connector. The optical interface uses a 12-fiber MTP/MPO connector. This module incorporates FIBERSTAMP proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

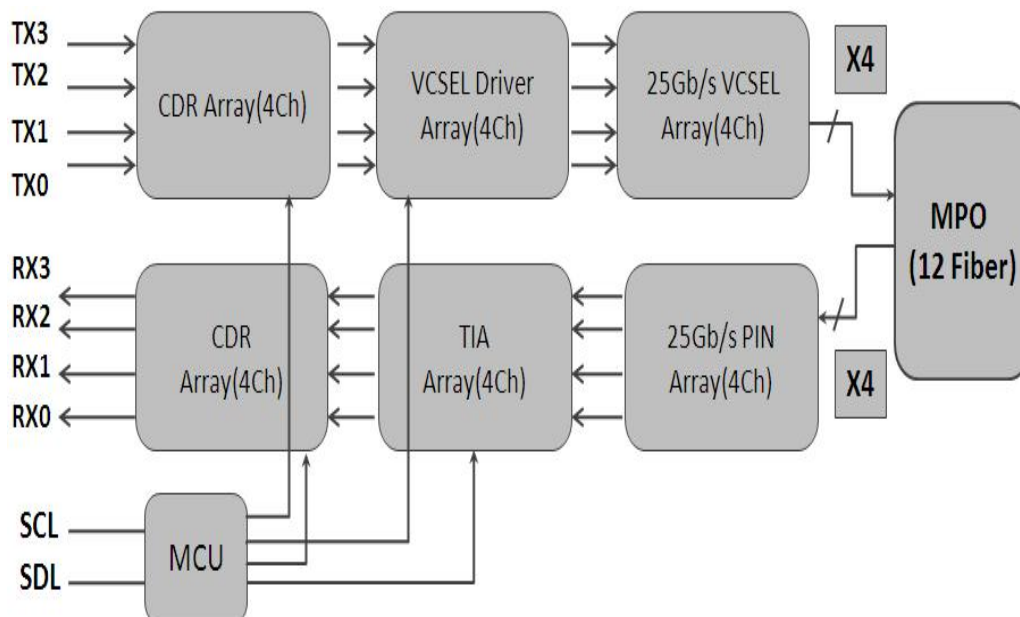


Figure 1. Module Block Diagram



The 100GBASE-SR4 QSFP28 is a parallel transceiver with the key technique of VCSEL and PIN array package, and can be contacted through I2C system.

### Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Tc	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

### Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tc	0		70	°C
Data Rate Per Lane	fd		25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	Pm			2	W
Fiber Bend Radius	Rb	3			cm

### Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude1	$\Delta V_{in}$	300		1100	mVp-p
Differential Output Voltage Amplitude2	$\Delta V_{out}$	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER		$5 \times 10^{-5}$		
Input Logic Level High	V <sub>IH</sub>	2.0		Vcc	V
Input Logic Level Low	V <sub>IL</sub>	0		0.8	V
Output Logic Level High	V <sub>OH</sub>	Vcc-0.5		Vcc	V
Output Logic Level Low	V <sub>OL</sub>	0		0.4	V

**Note:**

Differential input voltage amplitude is measured between TxnP and TxnN.

Differential output voltage amplitude is measured between RxnP and RxnN.



### Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
<b>Transmitter</b>					
Center Wavelength	$\lambda_c$	840	850	860	nm
RMS Spectral Width	$\Delta\lambda$			0.6	nm
Average Launch Power (each lane)	P <sub>out</sub>	-8.4		2.4	dBm
Optical Modulation Amplitude (each lane)	OMA	-6.4		3	dBm
Transmitter and Dispersion Eye Closure (each lane)	TDEC			4.3	dB
Extinction Ratio	ER	3			dB
Average Launch Power of OFF Transmitter (each lane)	P <sub>off</sub>			-30	dB
Eye Mask Coordinates1: X1, X2, X3, Y1, Y2, Y3		{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}			
<b>Receiver</b>					
Center Wavelength	$\lambda_c$	840	850	860	nm
Stressed Receiver Sensitivity in OMA2				-5.2	dBm
Average Power at Receiver Input (each lane)		-10.3		2.4	dBm
Receiver Reflectance	RR			-12	dB
LOS Assert	LOSA	-30			dBm
LOS De-Assert – OMA	LOSD			-7.5	dBm
LOS Hysteresis	LOSH	0.5			dB

**Note:**

Hit Ratio =  $5 \times 10^{-5}$

Measured with conformance test signal at TP3 for BER= $10^{-5}$

### Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground1
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground1
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground1
8	LVTTL-I	MODSEL	Module Select2
9	LVTTL-I	ResetL	Module Reset2
10		VCCR <sub>x</sub>	+3.3V Receiver Power Supply
11	LVC MOS-I	SCL	2-wire Serial interface clock2



Pin	Logic	Symbol	Name/Description
12	LVC MOS-I/O	SDA	2-wire Serial interface data2
13		GND	Module Ground1
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground1
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground1
20		GND	Module Ground1
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground1
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground1
27	LV TTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LV TTL-O	IntL	Interrupt output, should be pulled up on host board2
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LV TTL-I	LPMoDe	Low Power Mode2
32		GND	Module Ground1
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground1
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground1

**Note:**

Module circuit ground is isolated from module chassis ground within the module.

Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.



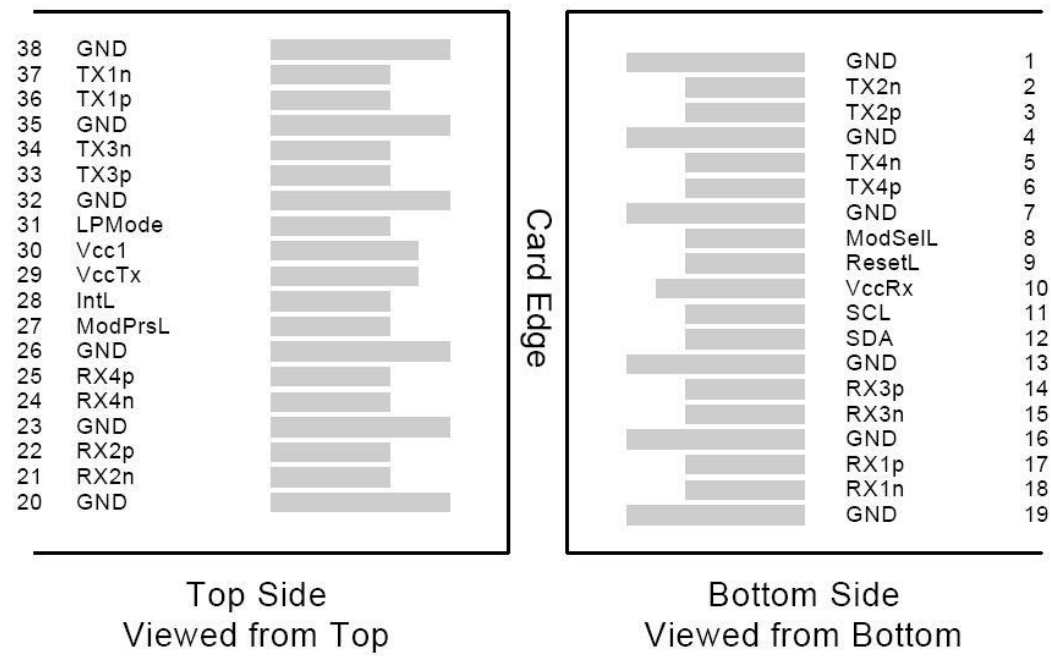


Figure 2. Electrical Pin-out Details

**ModSel Pin**

The ModSel is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSel allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSel is "High", the module will not respond to any 2-wire interface communication from the host. ModSel has an internal pull-up in the module.

**ResetL Pin**

Reset. LPMode\_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time ( $t_{init}$ ) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset ( $t_{init}$ ) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

**LPMode Pin**

FIBERSTAMP QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

**ModPrsL Pin**

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

**IntL Pin**

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

**Power Supply Filtering**

The host board should use the power supply filtering shown in Figure 3.

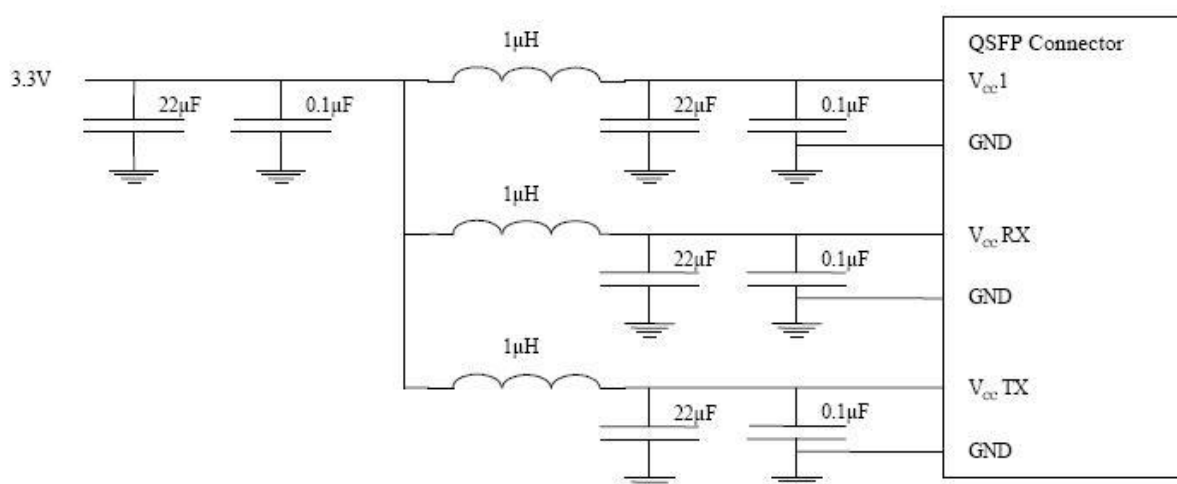
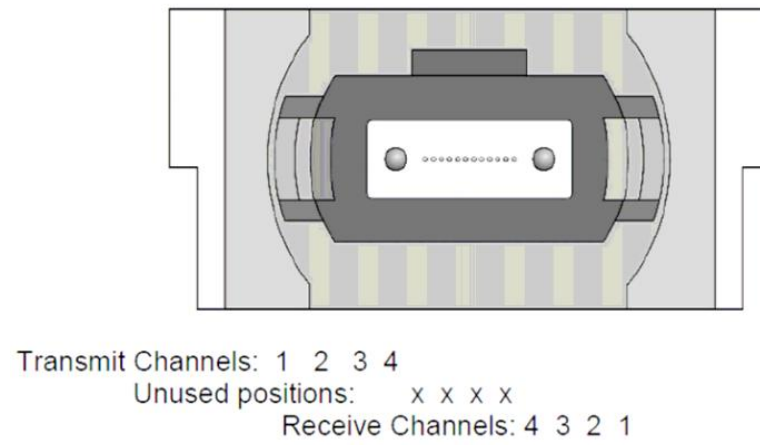


Figure 3. Host Board Power Supply Filtering

**Optical Interface Lanes and Assignment**

The optical interface port is a male MPO connector. The four fiber positions on the left as shown in Figure 4, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.



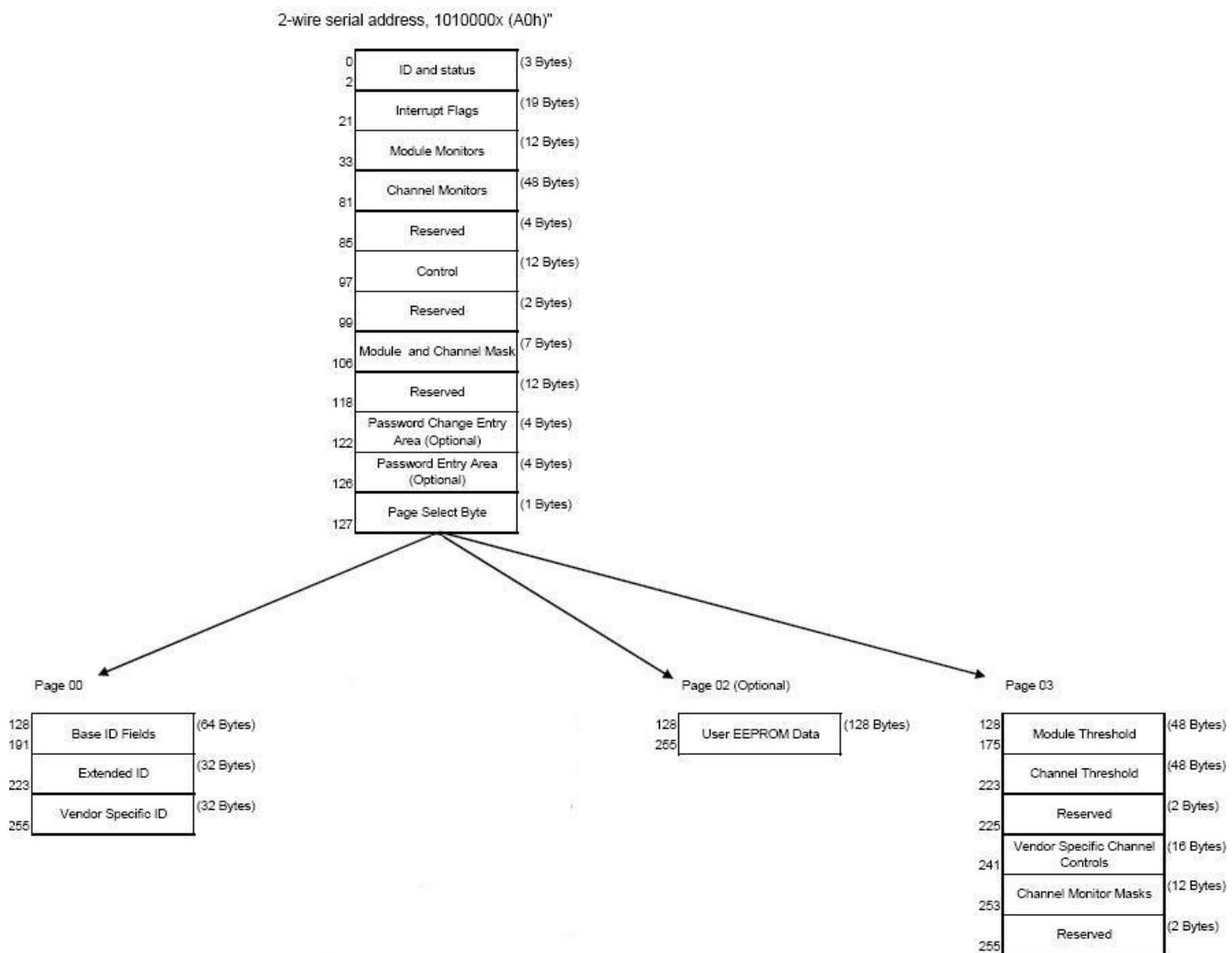
**Figure 4. Optical Receptacle and Channel Orientation**

**DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)**

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP28 transceivers. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.



**Figure 5. QSFP28 Memory Map**



Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mb/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125 μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand <sup>†</sup>
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00. Page 03 upper memory please see SFF-8436 document.



Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMMode Assert Time	ton_LPMMode	100	µs	Time from assertion of LPMMode (Vin: LPMMode=VIH) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout: IntL=VOL
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read3 operation of associated flag until Vout: IntL=VOH. This includes deassert times for Rx LOS, Tx Fault and other
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntL operation resumes
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set4 until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note :

Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.

Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.

Measured from falling clock edge after stop bit of read transaction.

Measured from falling clock edge after stop bit of write transaction.

Mechanical Dimensions

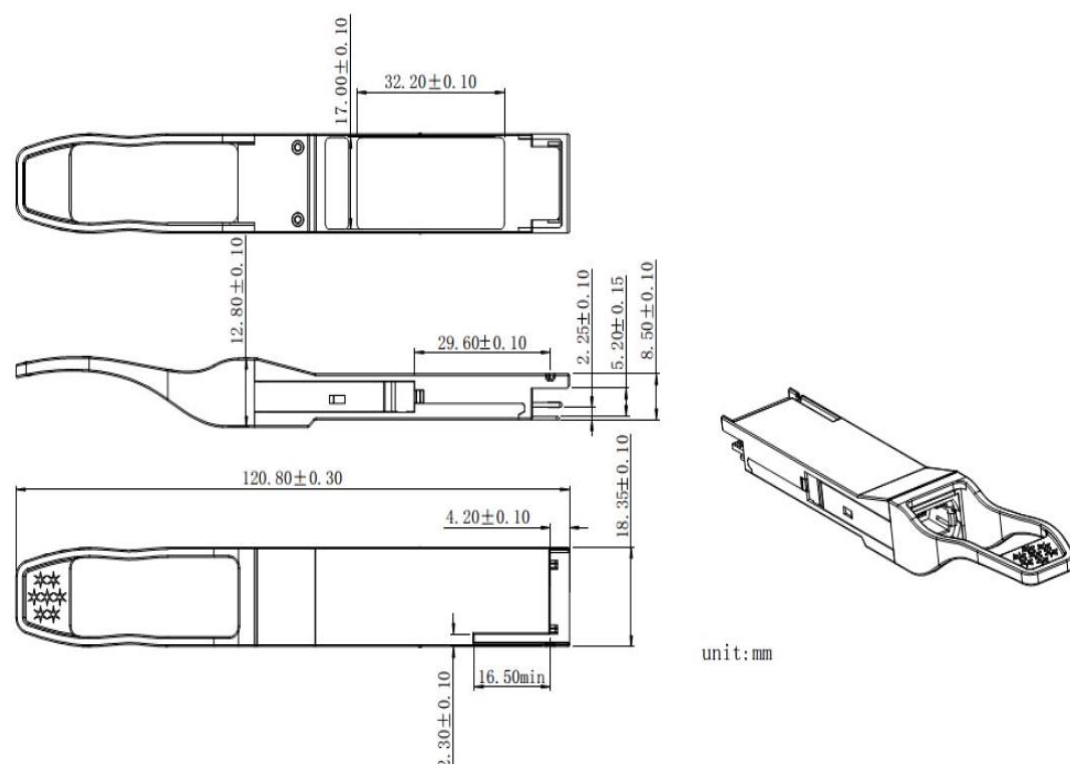


Figure 9. Mechanical Specifications





### Regulatory Compliance

FIBERSTAMP FEG-100S4M10C transceivers are Class 1 Laser Products. They meet the requirements of the following standards.

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032 : 2015 EN55035 : 2017
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

### References

1. QSFP28 MSA
2. Ethernet 100GBASE-SR4 IEEE802.3bm

### Ordering Information

Part Number	Product Description
FEG-100S4M10C	QSFP28 SR4, 103.125Gb/s, 850nm, 100m, MMF, MTP/MPO

### CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

### Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by FIBERSTAMP before they become applicable to any particular order or contract. In accordance with the FIBERSTAMP policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of FIBERSTAMP or others. Further details are available from any FIBERSTAMP sales representative.

