



100Gbps QSFP28 PSM4 O-band DWDM Optical Transceiver Module

FEG-1000xK40C

Features

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 26Gbps per channel
- 4 channels O-band DML DWDM
- Compliant to ITU-T 694.1
- 4 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <5W
- Hot Pluggable QSFP form factor
- Up to 40km reach for G.652 SMF with external Mux/Demux,SOA
- Up to 10km reach for G.652 SMF without external SOA
- Single male MPO(APC 8-degree) connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS compliant(lead free)

Applications

- 100G Ethernet Metro-Access over DWDM
- P to P Access Network

Description

The FIBERSTAMP Technologies FEG-1000xK40C is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP28 PSM4 for 100G or 40 Ethernet Metro-Access over DWDM applications. The transceiver is a high performance module for data communication and interconnect applications. It integrates four data lanes in each direction with 104 Gbps bandwidth. Each lane can operate at 26Gbps up to 40km over G.652 SMFwith external Mux/Demux,SOA.The electrical interface uses a 38 contact edge type connector. The optical interface uses a 12 fiber MTP (MPO) connector. This module incorporates FIBERSTAMP Technologies proven circuit and Optical technology to provide reliable long life, high performance, and consistent service.







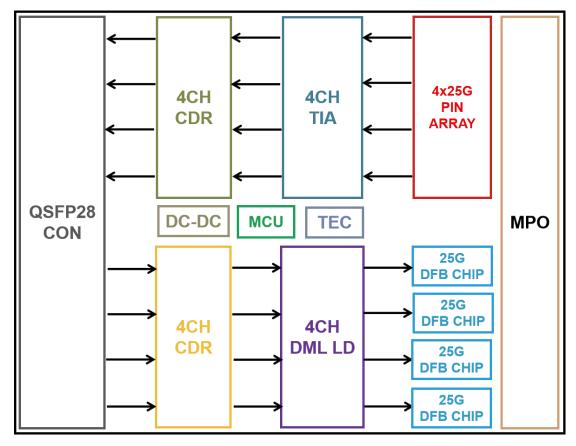


Figure 1. Module Block Diagram

100Gb/s QSFP28 PSM4 O-band DWDM is one kind of parallel transceiver. DFB and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Тор	0	70	°C
Humidity(non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Operating Case temperature	Тса	0		70	°C	
Data Rate Per Lane	fd		25.78125		Gbps	
Humidity	Rh	5		85	%	
Power Dissipation	Pm			5	W	
Link Distance with G.652	D			40	km	1

Note:

1.Requires a DWDM line system with amplification and dispersion management.





Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	190		700	m∨p-p
Differential output voltage amplitude	ΔVout	300		850	mVp-p
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note:

- 1. Differential input voltage amplitude is measured between TxnP and TxnN.
- 2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
		Transmitt	er			
Centre Wavelength	λс		per ITU-T 694.	1	nm	-
Side Mode Suppression Ratio	SMSR	30	-		dB	-
Average launch power, each lane	PAVG	-1		6	dBm	-
TDP each lane	TDP			2.9	dB	
Extinction Ratio	ER	4	-	-	dB	-
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-20	dB	
Average launch power of OFF transmitter, each lane	POFF			-30	dBm	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.31,0.4	4,0.45,0.34,0.38	.0.4}		Hit Ratio = 5x10-5
		Receive	er			
Centre Wavelength	λс	1260		1360	nm	-
Damage Threshold, each lane	THd	5.5			dBm	1
Average Receive Power, each lane		-10.6		4.5	dBm	
Receive power, each lane (OMA)				4.5	dBm	
Receiver Reflectance	RR			-26	dBm	
Receiver Sensitivity (OMA), each lane	SEN			-8.6	dBm	2





Parameter	Symbol	Min	Typical	Max	Unit	Notes
LOS Assert	LOSA		-18		dBm	-
LOS De-Assert – OMA	LOSD		-15		dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note:

- 1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
- 2. Sensitivity is specified at $1x10^{-12}$ BER at 25.78125 Gb/s.

O-band λc Wavelength Grid

	TX1		TX2		TX3		TX4	
Product Code	Ch.	Frequency	Ch Na	Frequency			Ch Na	Frequency
	No.	(THz)	Ch. No.	(THz)	Ch. No.	(THz)	Ch. No.	(THz)
FEG-10001K40C	01	233.6	02	233.45	03	233.3	04	233.15
FEG-10005K40C	05	233	06	232.85	07	232.7	08	232.55
FEG-100010K40C	10	232.25	11	232.1	12	231.95	13	231.8
FEG-100014K40C	14	231.65	15	231.5	16	231.35	17	231.2

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	





Pin	Logic	Symbol	Name/Description	Ref.
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

- 1. Module circuit ground is isolated from module chassis ground within the module.
- 2. Open collector; should be pulled up with 4.7k 10k ohms on host board to a voltage between 3.15V and 3.6V.

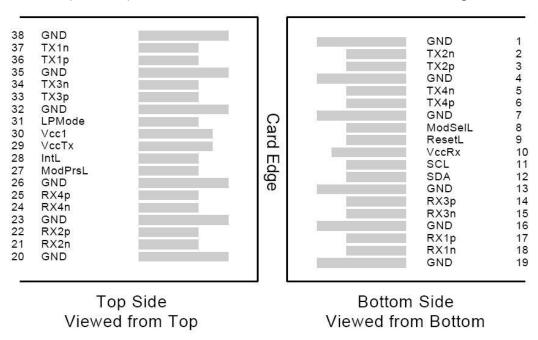


Figure 2. Electrical Pin-out Details





ModSell Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

FIBERSTAMP QSFP28 PSM4 operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

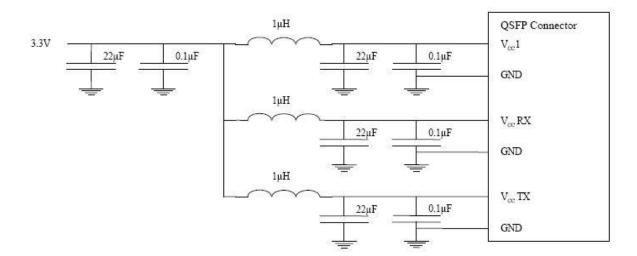


Figure 3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The 12 fiber MPO optical lane assignments are shown in Figure 4. The four transmit and four receive optical lanes of





PSM4 shall occupy the positions depicted in Figure 8 with looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The central 4 fibers may be physically present.

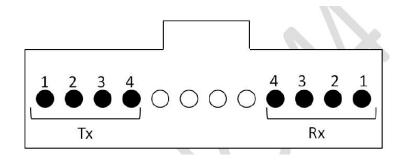


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP28 PSM4. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

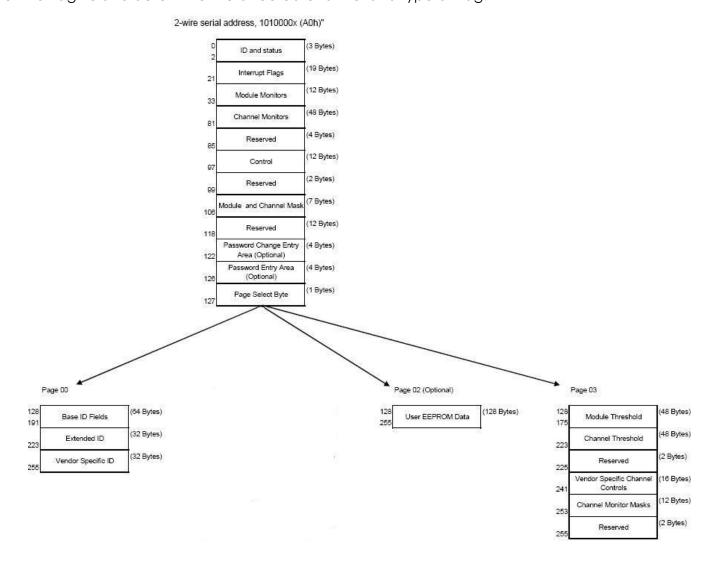


Figure 5. QSFP Memory Map





Byte Address	Description	Туре
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Туре
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 µm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 µm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125µm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand [†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tof. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure8. Page 00 Memory Map





Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 and SFF-8636 document.

SFF-8636 definiens

TX AND RX CDR LOL indicator (Byte 5)

L.	Tr.	(6	indicacori chamer 2	30	(6		(6
5	7	L-Tx4 L0L	Latched TX CDR LOL indicator, ch 4	0	0	0	0
	6	L-Tx3 LOL	Latched TX CDR LOL indicator, ch 3	0	0	0	0
	5	L-Tx2 L0L	Latched TX CDR LOL indicator, ch 2	0	0	0	0
	4	L-Tx1 L0L	Latched TX CDR LOL indicator, ch 1	0	0	0	0
	3	L-Rx4 LOL	Latched RX CDR LOL indicator, ch 4	0	0	0	0
	2	L-Rx3 LOL	Latched RX CDR LOL indicator, ch 3	0	0	0	0
	1	L-Rx2 LOL	Latched RX CDR LOL indicator, ch 2	0	0	0	0
	0	L-Rx1 LOL	Latched RX CDR LOL indicator, ch 1	0	0	0	0

TX AND RX CDR BYPASS CONTROL (Byte 98)

98	7	Tx4_CDR_control	Channel 4 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	6	Tx3_CDR_control	Channel 3 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	5	Tx2_CDR_control	Channel 2 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	4	Tx1_CDR_control	Channel 1 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	3	Rx4_CDR_control	Channel 4 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	2	Rx3_CDR_control	Channel 3 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	1	Rx2_CDR_control	Channel 2 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	0	Rx1_CDR_control	Channel 1 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0

TABLE 6-33 OUTPUT DIFFERENTIAL AMPLITUDE CONTROL (PAGE 03H BYTES 238-239)

Value	Receiver Outpu No Output Equ		
	Nominal	Units	
1xxxb	Reserved		
0111b	Reserved	mV(P-P)	
0110b	Reserved mV(P-P		
0101b	Reserved mV(P-F		
0100b	Reserved	mV(P-P)	
0011b	600-1200	mV(P-P)	
0010b	400-800	mV(P-P)	
0001b	300-600 mV(P-P)		
0000b	100-400	mV(P-P)	

TABLE 6-34 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

Value	Transmitter Inpu	it Equalization
99	Nominal	Units
11xxb	Reserved	
1011b	Reserved	
1010b	10	dB
1001b	9	dB
1000b	8	dB
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No EQ





TABLE 6-35 OUTPUT EMPHASIS CONTROL (PAGE 03H BYTES 236-237)

Value	Receiver Outp At nominal Out	
	Nominal	Units
1xxxb	Reserved	
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2 dB	
0001b	1 dB	
0000b	0 No Empha	

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on ¹ , hot plug or rising edge of Reset until the module is fully functional ²
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on ¹ until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on ¹ to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional ²
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read ³ operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set ⁴ until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared ⁴ until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module

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Parameter	Symbol	Max	Unit	Conditions
				does not respond to data transmission over the
				2-wire serial bus
Power_over-ride or	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power
Power-set Assert Time				consumption enters lower Power Level
Power_over-ride or	toff Pdown	200		Time from P_Down bit cleared4 until the module is
Power-set Deassert Time		300	ms	fully functional3

Note:

- 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
- 2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
- 3. Measured from falling clock edge after stop bit of read transaction.
- 4. Measured from falling clock edge after stop bit of write transaction.

Mechanical Dimensions

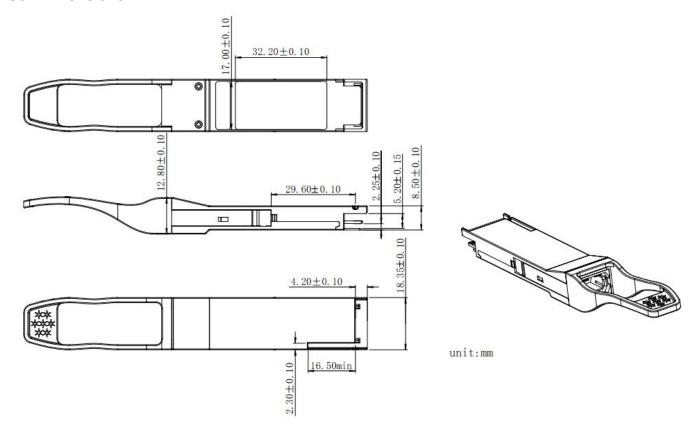
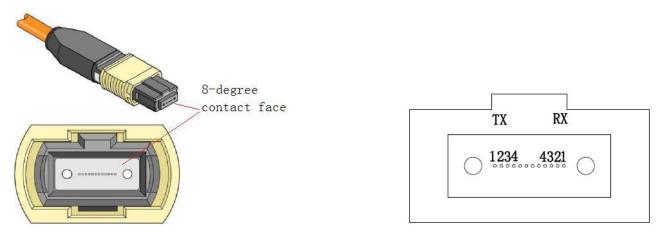


Figure 9. Mechanical Specifications



Female MPO(APC 8-degree) connector for this module

Regulatory Compliance

FIBERSTAMP FEG-1000xK40C QSFP28 transceivers are Class 1 Laser Products. They meet the requirements of the following standards:

Feature	Standard
	IEC 60825-1:2014 (3 rd Edition)
Laser Safety	IEC 60825-2:2004/AMD2:2010
	EN 60825-1-2014





Feature	Standard		
	EN 60825-2:2004+A1+A2		
	EN 62368-1: 2014		
Electrical Safety	IEC 62368-1:2014		
	UL 62368-1:2014		
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863		
	EN55032: 2015		
CE EMC	EN55035: 2017		
CE EMC	EN61000-3-2:2014		
	EN61000-3-3:2013		
FCC	FCC Part 15, Subpart B		
FCC	ANSI C63.4-2014		

References

- 1. SFF-8436 QSFP+
- 2. 100G PSM4 MSA



Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description				
FFG-1000xK40C	100Gb/s QSFP28 PSM4 O-band DWDM, MPO Connector, reach 40km on G.652,				
1 LG-1000XX40C	0~70°C				

Important Notice

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