100G / 200G CFP2 DCO Optical Transceiver

FVN-200T50W10CN / FVN-100T50W12CN

Features

- 100G CFP2-DCO coherent optical module operating up to 112.30 Gbps
- 200G CFP2-DCO coherent optical module operating up to 211.45 Gbps
- PM-QPSK (100G) and PM-16QAM (200G) modulation formats
- 100GE, OTU4, OTUC1 and OTUC2 services
- Electrical interfaces OTL4.4, OTLC1.4, CAU-I4, OTLC2.8 and CEI-28G-MR
- CFP2 MSA Hardware Specification 1.0 with modifications compliant
- CFP MSA Management Interface Specification 2.2 with modifications compliant
- Near-end / remote-end data loopback
- Hot-pluggable CFP2 form factor
- Maximum power consumption: 24 W

Applications

- 100GbE IEEE 802.3bj;
- ITU-T G.709/Y.1331 for Optical transport network
- Switch to switch interface or Switch to router interface
- Access, Metro, Long-haul Ethernet DWDM Networks

Description

The 100G / 200G CFP2-DCO coherent optical module uses a 104-pin CFP2-MSA electrical connector for connecting the host card. Figure 1-1 shows the picture of this module.

The optical module consists of three functional parts: TX module, RX module and control module. All the control interface pins are provided by an internal microcontroller. This microcontroller can also be used for modulator control, software management, and alarm/performance event reporting. Below picture shows the block diagram of the 100G / 200G CFP2-DCO coherent optical module.

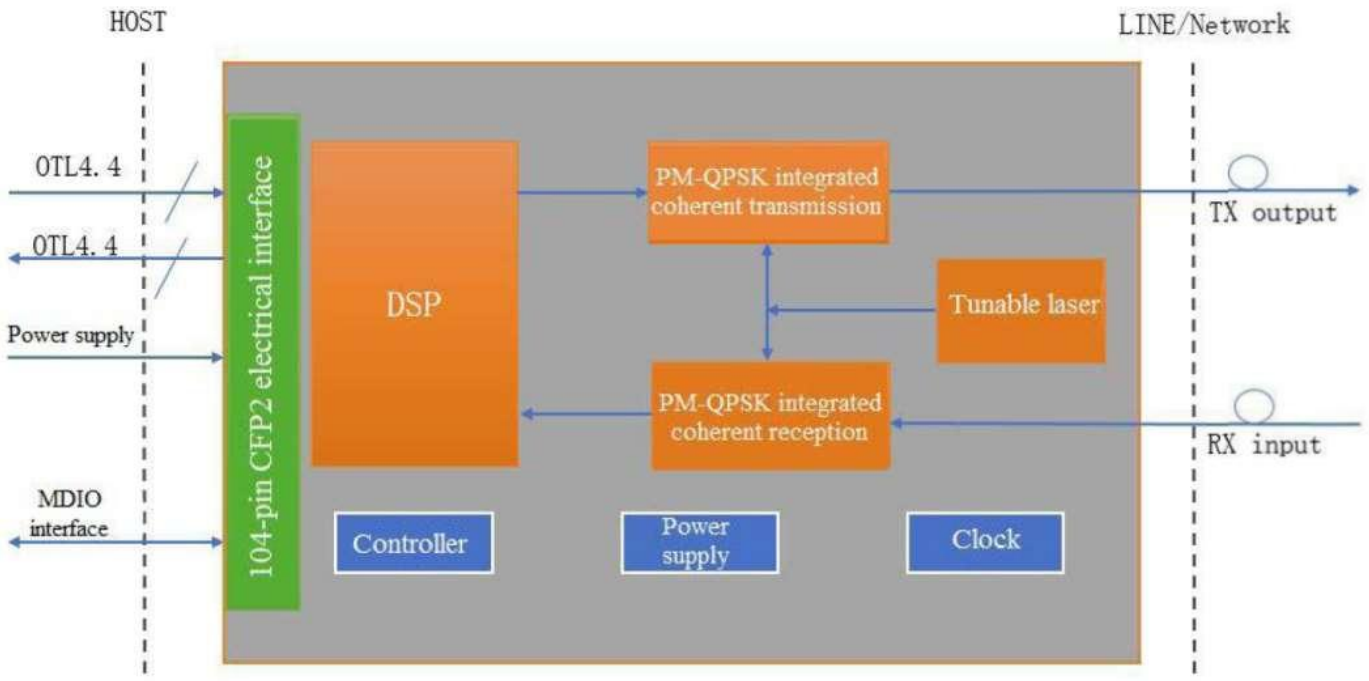


Figure 1: Module Block Diagram

100G Optical Port

Parameter	Value
Network lane, modulation format	PM-QPSK
Optical channels	96
Grid spacing	50 GHz
Frequency range	191.3 to 196.05 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
DGD tolerance	50 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	12.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 W Maximum: 24 W

200G Optical Port

Parameter	Value
Network lane, modulation format	PM-16QAM
Optical channels	96
Grid spacing	50 GHz
Frequency range	191.3 to 196.05 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6.5 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	18.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 W Maximum: 24 W

Electrical Characteristics

Power Supply Specification

The 100G / 200G CFP2 coherent optical module is powered by an independent 3.3 V power supply on the host. All voltages are tested at the connector interfaces. Table 4-3 describes the power supply requirements.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
3.3V DC power supply voltage	VCC	3.2	3.3	3.4	V	±5%
3.3VDC power supply current	ICC	-	-	7.3	A	Note 1 & 2
Power supply noise	Vrip	-	-	2	%p-p	DC - 1 MHz
				3		1 - 10 MHz
Power consumption	Pw_class 4	-	22	24	W	200G mode

Note:

1. The Min. and Max. values apply to the full temperature range at the EOL of the module. Typical values (Typ.)are defined at the BOL of the module, with operating temperature at 25ºC and expected power supplied.
2. The maximum current of each pin cannot exceed 1.3 A.
3. The Max. value of Icc is for design reference, and the expected working current cannot exceedPw_normal/Vcc.

High-Speed Electrical Interface Specifications

The transmitter data signal complies with the CEI-28G-MR low swing standards.

The receiver data signal complies with the CEI-28G-MR standards.

Reference Clock (REFCLK): The host does not need to provide a reference clock (REFCLK) for the 100G / 200G CFP2-DCO coherent optical module, because a 622.08M local clock is integrated in the 200G CFP2-DCO coherent optical module.

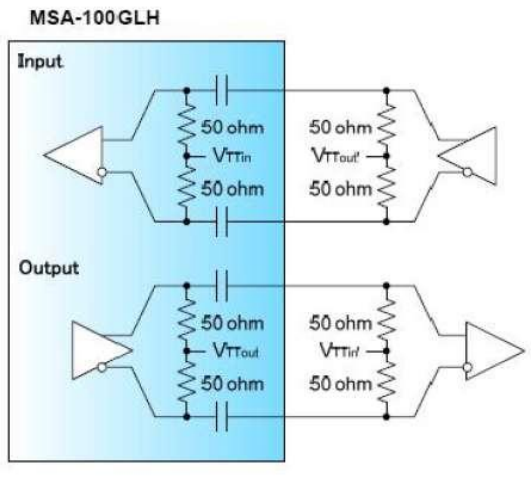


Figure 2: High-Speed I/O for Data and Clocks

Transmitter Monitor Clock (TXMCLK)

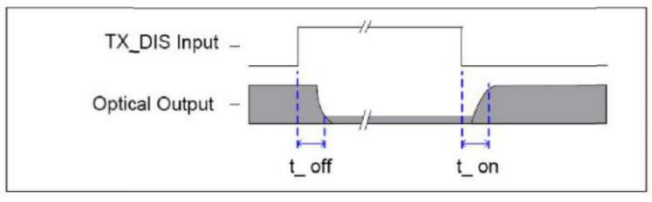
The transmitter of the 100G / 200G CFP2-DCO coherent optical module provides a monitoring clock TXMCLK, which is mainly used as a reference for monitoring optical signals at the transmitter. The clock can be used to trigger a high-speed sampling oscilloscope

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Impedance	Zd	80	100	120	Ω	-
Transmitter monitor clock frequency (TXMCLK)	-	-	1 / 48	7.3	Hz	The frequency is 1/48 the symbol rate of the transmitter's optical signal.
TXMCLK differential voltage	VDIFFTX	500	-	1000	mV	Differential peak-to-peak voltage

Control Pins (non-MDIO) Functional Description

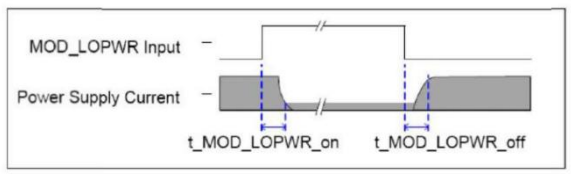
TX_DIS (Transmitter Disable)

TX_DIS is an input pin which receives signals from the host and operates in the logic high state. When TX_DIS is logic high, the output optical signal inside the optical module is turned off. When TX_DIS is logic low, the output optical signal inside the optical module is turned on. The symbol "t_on" is the turn-on time and "t_off" is the turn-off time. Below picture shows the timing diagram.



MOD_LOPWR (Module Low Power)

MOD_LOPWR is an input pin which receives signals from the host and works in the logic high state. When MOD_LOPWR is logic high, the optical module works at low power consumption and remains in this mode. When MOD_LOPWR is pulled down, the optical module is initialized to a high power consumption state, that is, the normal operation mode. In low power consumption mode, the optical module communicates through the MDIO management interface, and its maximum power consumption does not exceed 2 W. Below picture shows the values of "t_MOD_LOPWR_on" and "t_ MOD_LOPWR_off".



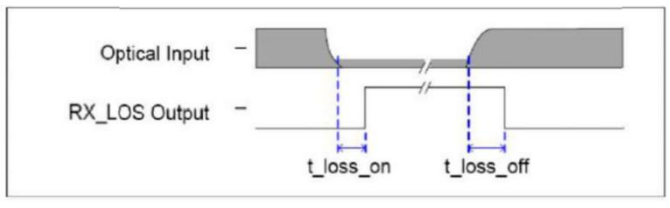
MOD_RSTn (Module Reset)

MOD_RSTn is an input pin which receives signals from the host and works in the logic low state. When MOD_RSTn is pulled low, the optical module is in the reset state. When MOD_RSTn is logic high, the optical module exits the reset mode and starts power-on initialization.

Alarm Pins (non-MDIO) Functional Description

RX_LOS (Receiver Loss of Signal)

RX_LOS is an output pin which transmits signals to the host and works at the logic high state. When RX_LOS is logic high, the optical power received by the optical module is too low. Figure 4-4 shows the timing diagram for RX_LOS.



MOD_ABS (Module Absent)

MOD_ABS is an output pin which transmits signals from the inside of the module to the host. This pin is pulled up on the host and pulled down to the ground inside the module. When the optical module is inserted into the host, MOD_ABS is logic low, meaning that the module is present. When the optical module is absent on the host, MOD_ABS is logic high, meaning that the module is absent.

Control and Alarm Descriptions

Timing Parameters for Control and Alarm Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter Disabled (TX_DIS high)	t_off	-	-	1	ms
Transmitter Enabled (TX_DIS low)	t_on	-	-	25	s
MOD_LOPWR assert	t_MOD_LOPWR_assert	-	-	25	s
MOD_LOPWR deassert	t_MOD_LOPWR_deassert	-	-	25	s

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver Loss of Signal Assert Time	t_loss_on	-	-	1	ms
Receiver Loss of Signal De-assert Time	t_loss_off	-	-	15	ms
Initialization time from Reset	t_initialize	190	-	220	s

3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	3.2	3.3	3.4	V
Input high voltage	VIH	2	-	VCC+0.3	V
Input low voltage	VIL	-0.3	-	0.8	V
Input leakage current	IIN	-10	-	10	μA
Output high voltage (IOH =-100 μA)	VOH	VCC-0.2	-	-	V
Output low voltage (IOL =100 μA)	VOL	-	-	0.2	V

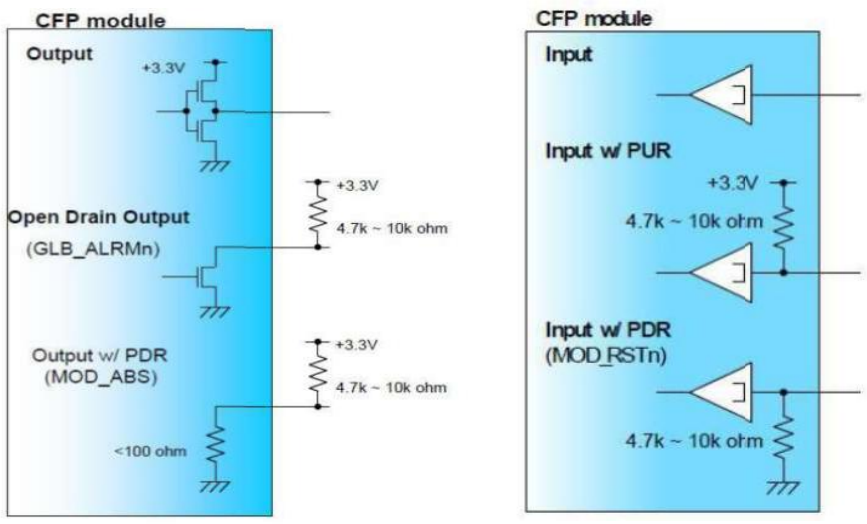


Figure 3: Reference 3.3 V LVCMOS Input / Output Termination

Management Data Input / Output (MDIO) Interface

The MDIO implementation is defined in IEEE 802.3 clause 45. The optical module supports a lane rate of up to 4 Mb/s. The MDIO of the optical module uses the 1.2 V LVCMOS logic level.

Management Data Clock (MDC) Interface Pins

The host defines that the maximum MDC rate can reach 4 MHz, so the maximum MDC rate that the optical module supports can reach 4 MHz.Below picture shows the timing diagram for the MDIO and MDC pins. The optical module should follow the minimum setup time "tsetup" and hold time "thold" requirements of the MDIO port supplementary protocol.

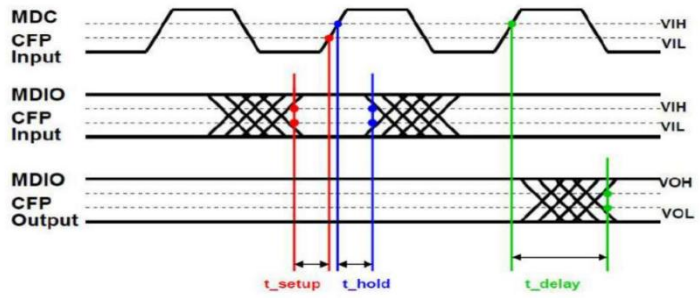


Figure 4: Timing Diagram for the MDIO & MDC Interfaces

Note: Tested on the MDIO & MDC pins of the optical module.

MDIO Physical Port Address Pins (PRTADRs)

The PRTADRs are used by the host system to assign addresses to all optical modules belonging to its management area. PREADR0 corresponds to the LSB of the physical port address bit. The host drives the physical port address line of 5pin to set the physical port address of the optical module by following the address protocol of the MDIO port. It is recommended that these physical port addresses should not change when the optical module is powered on.

1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input high voltage	VIH	0.84	-	1.5	V
Input low voltage	VIL	-0.3	-	0.36	V
Input leakage current	IIN	-100	-	100	µA
Output high voltage (IOH =-100 µA)	VOH	1	-	1.5	V
Output low voltage (IOL =100 µA)	VOL	-0.3	-	0.2	V
Output high current	IOH	-	-	-	mA
Output low current	IOL	+4	-	-4	mA
Input capacitance	Ci	-	-	10	pF

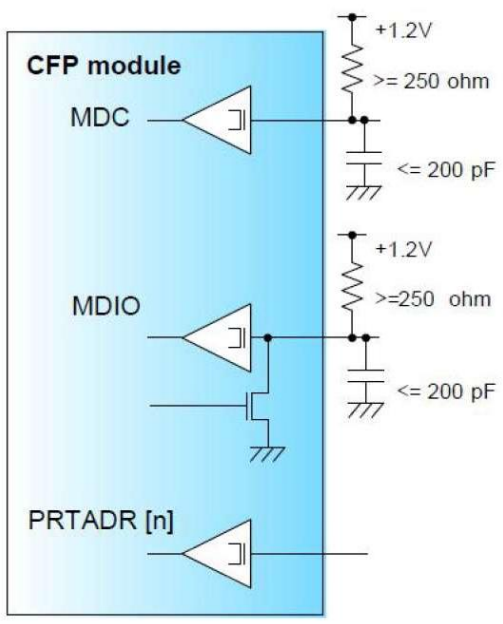


Figure 5: Reference MDIO Interface Termination

Operating Environment

Parameter	Min.	Max.	Unit
Storage temperature	-40	85	°C
Operating case temperature	0	70	°C
Relative humidity, operating(non-condensing)	5	85	%
Relative humidity, operating(short term < 96 hrs,non-condensing)	5	95	%
ESD sensitivity (HBM)		High-speed pins: 1000 Other pins: 2000	V
Parameter	Min.	Max.	Unit
Storage temperature	-40	85	°C
Operating case temperature	0	70	°C

Pin Assignment and Description

The electrical connection of 104pin includes four pairs of TX differential signals (these signals are the inputTXIs of the 100G module, which connect to the signal outputs of the card), four pairs of RX differentialsignals (these signals are the output RXOs of the CFP2 module, which connect to the signal inputs of thecard), a pair of 622 MHz reference clocks, a pair of monitoring clocks in Tx and Rx directions, control pins,alarm pins, MDIO communication related pins, GND and +3.3 V power supply. The +3.3 V power supplysupports a maximum overcurrent capacity of 1.3 A per pin.

PIN#	NAME	I/O	Logic	Description
1	GND			
2	*(TX_MCLKn) or Vendor_Out0n*	O	CML	For optical waveform testing or Module vendor output
3	*(TX_MCLKp) or Vendor_Out0p*	O	CML	For optical waveform testing or Module vendor output
4	GND			
5	Vendor_In0n	I	CML	Module vendor input. Vendor specific.
6	Vendor_In0p	I	CML	Module vendor input. Vendor specific.
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	Vendor_In1n	I	CML	Module vendor input
48	Vendor_In1p	I	CML	Module vendor input
49	GND			
50	*(RX_MCLKn) or Vendor_Out1n*	O	CML	For optical waveform testing or Module vendor output
51	*(RX_MCLKp) or Vendor_Out1p*	O	CML	For optical waveform testing or Module vendor output
52	GND			

	Top (4x25G)
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p

	Top (8x25G)
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	TX6n
90	TX6p
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	TX7n
81	TX7p
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND

68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

Mechanical Specifications

The mechanical dimensions of the 100G/200G CFP2-DCO coherent optical module. Max. dimensions (L×W×H): 107.5 mm× 42.5 mm×13.4 mm

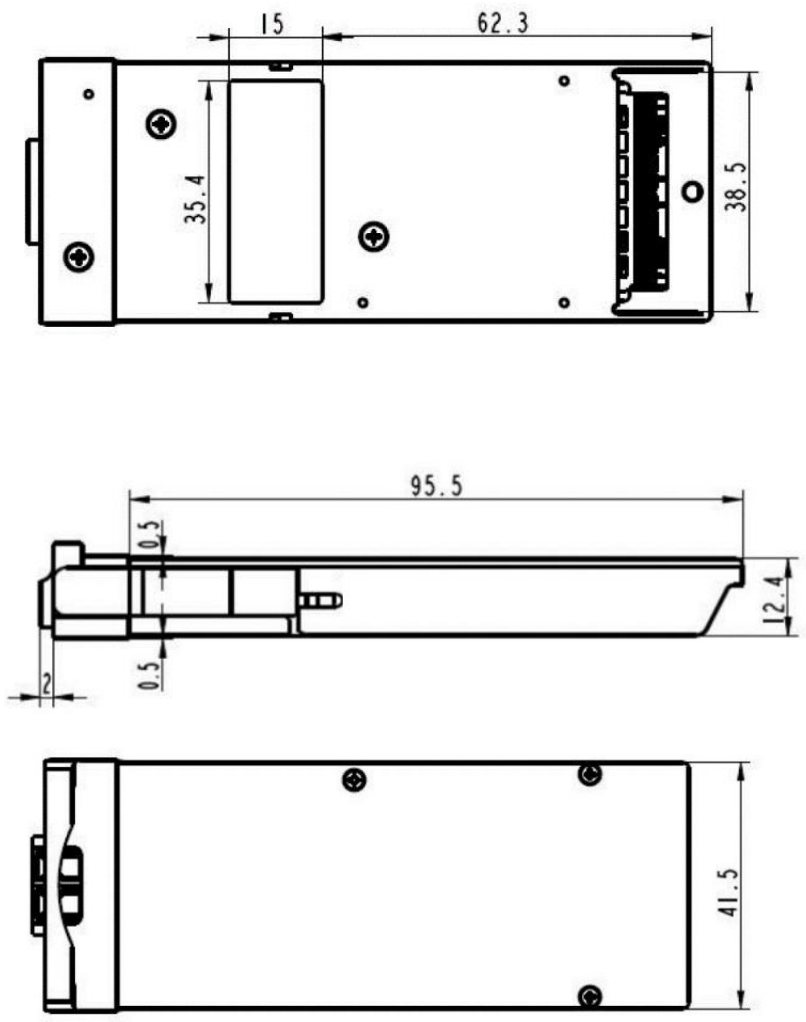


Figure 5: Mechanical dimensions

Regulatory Compliance

FIBERSTAMP 100G CFP2 DCO transponders are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition)
Environmental protection	2011/65/EU
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

Ordering information

Part Number	Product Description
FVN-200T50W10CN / FVN-100T50W12CN	CFP2 DCO, Tunable,C_band, 100G LH, 200G MR

References：

IEEE 802.3ba;

ITU-T G.709/Y.1331

RoHS 2.0 compliant (2011/65/EU, lead free)

CFP2-MSA-HW-Spec-rev1.0

CFP_MSA_MIS_V2p6r06a

CFP2_MSA_Module-Dimensions_APRIL07-10

CFP2_MSA_Host-Mechanical-drawings

OIF-MSA-100GLH-EM-02.1

Regulation (EC) No.1907/2006(REACH)

Tested in accordance with Telcordia GR-468

IEC 60825-1:2014

EN 60825-1:2014

EN 60825-2:2004+A1+A2

FDA CDRH 21 CFR 1040

EN 60950-1:2006+A11+A1+A12+A2

EN 62368-1: 2014+A11:2017

UL 60950-1 & CAN/CSA C22.2 No. 60950-1

UL 62368-1:2014

IEC 60950-1:2005+AMD1:2009+AMD2:2013

IEC 62368-1:2014

GB 4943.1-2011

47 CFR FCC Part 15 Subpart B

EN 55032:2015

EN 55024:2010+A1:201

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Important Notice

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